



# NETAŞ NCS6742G N4

## Rack Server

## Hardware Description

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Version: R1.8

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## **Revision History**

| <b>Revision No.</b> | <b>Revision Date</b> | <b>Revision Reason</b>   |
|---------------------|----------------------|--|
| R1.8                | 2025-10-16           | Updated "1.2.2 Switch Boards".   |
| R1.7                | 2025-06-30           | Updated "1.2.2 Switch Boards".   |
| R1.6                | 2025-05-31           | Updated "9.3 Switch Boards".   |
| R1.5                | 2025-03-31           | Updated "6.2 PCIe Card Slots and Descriptions".  |
| R1.4                | 2025-01-10           | <ul style="list-style-type: none"><li>Added " 1 Product Structure".</li><li>Updated "5.1 OCP NIC".</li></ul> |

| <b>Revision No.</b> | <b>Revision Date</b> | <b>Revision Reason</b>  |
|---------------------|----------------------|---|
|                     |                      | <ul style="list-style-type: none"><li>• Updated "5.2 PCIe NIC".</li></ul> |
| R1.3                | 2024-11-26           | Updated "4.2 PCIe NIC".   |
| R1.2                | 2024-07-29           | Added "9 Cables".   |
| R1.1                | 2024-06-21           | Updated "4.2 PCIe NIC".   |
| R1.0                | 2023-12-11           | First edition.  |

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# About This Manual

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## Purpose

This manual describes the hardware configurations of the NCS6742G N4 rack server so that you can learn about detailed information about the server's components including the [CPUs](#), [DIMM](#)s, storage, network, [I/O](#) expansion, power modules and fan units.

## Intended Audience

This manual is intended for:

- Network planning engineers
- Hardware installation engineers
- On-site maintenance engineers

## What Is in This Manual

This manual contains the following chapters:

|                              |   |
|------------------------------|---|
| Chapter 1, Product Structure | Describes the physical structure and logical structure of the NCS6742G N4.                                  |
| Chapter 2, CPU               | Describes the positions of CPUs in the NCS6742G N4 and the recommended CPU configurations.                  |
| Chapter 3, DIMM              | Describes the DIMM slots in the NCS6742G N4 and the supported DIMM configurations.                          |
| Chapter 4, Storage           | Describes the hard disk slots of the NCS6742G N4 and the supported hard disk configurations.                |
| Chapter 5, Network           | Describes the positions of the onboard <a href="#">NIC</a> and <a href="#">OCP</a> card in the NCS6742G N4. |
| Chapter 6, I/O Expansion     | Describes the <a href="#">PCIe</a> slots of the NCS6742G N4 and the supported PCIe card configurations.     |
| Chapter 7, Power Module      | Describes the positions of power modules in the NCS6742G N4 and the supported power module configurations.  |
| Chapter 8, Fan Unit          | Describes the positions of fan units in the NCS6742G N4 and the supported fan unit configurations.          |
| Chapter 9, Boards            | Describes the configurations of the mainboard and hard disk backplanes in the NCS6742G N4.                  |

|                                   |  |
|-----------------------------------|--|
| Chapter 10, Cables                | Describes the functions, structures, and usage of cables used by the NCS6742G N4.            |
| Chapter 11, Anti-Intrusion Sensor | Describes the functions and position of the anti-intrusion sensor in the NCS6742G N4 server. |

## Conventions

This manual uses the following conventions:

|   |   |
|---|---|
|    | <p>Danger: indicates an imminently hazardous situation. Failure to comply will result in death or serious personal injury.</p> <p>Warning: indicates a potentially hazardous situation. Failure to comply can result in death or serious personal injury.</p> <p>Caution: indicates a potentially hazardous situation. Failure to comply can result in moderate or minor personal injury.</p> |
|    | <p>Notice: indicates equipment or environment safety information. Failure to comply can result in equipment damage, data loss, equipment performance degradation, environmental contamination, or other unpredictable results.</p> <p>Failure to comply will not result in personal injury.</p>   |
|  | <p>Note: provides additional information about a topic.</p>   |

# Chapter 1

# Product Structure

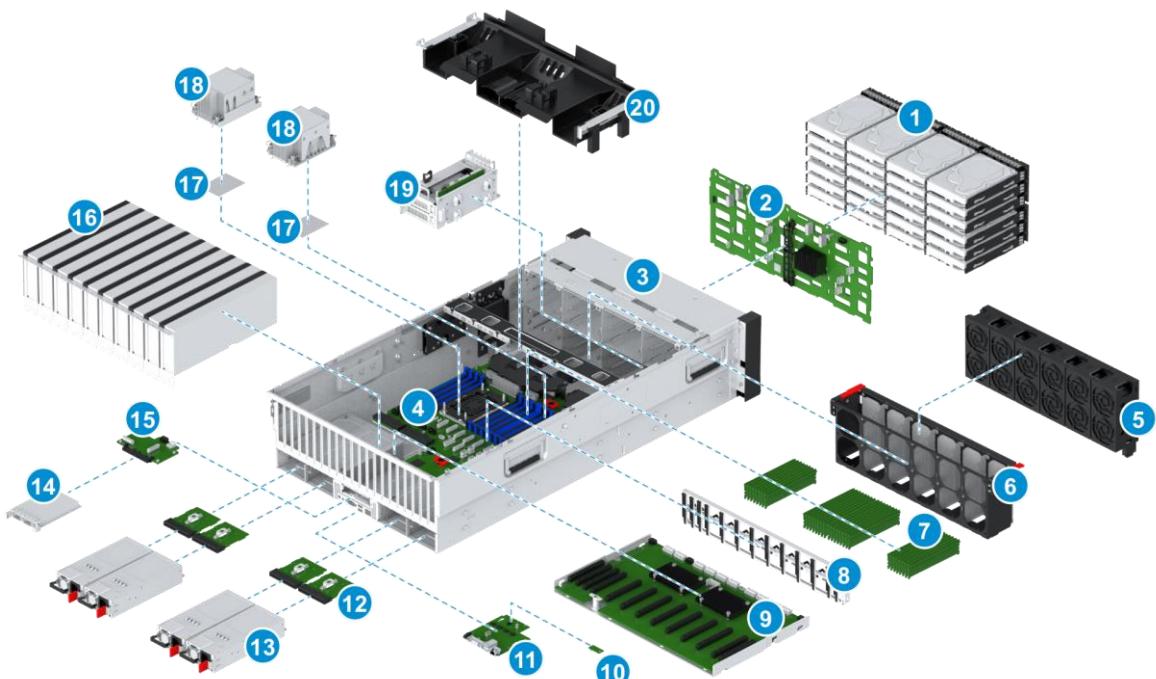
## Table of Contents

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## 1.1 Physical Structure

Figure 1-1 shows the internal components of the NCS6742G N4 server.

**Figure 1-1 Internal Layout**



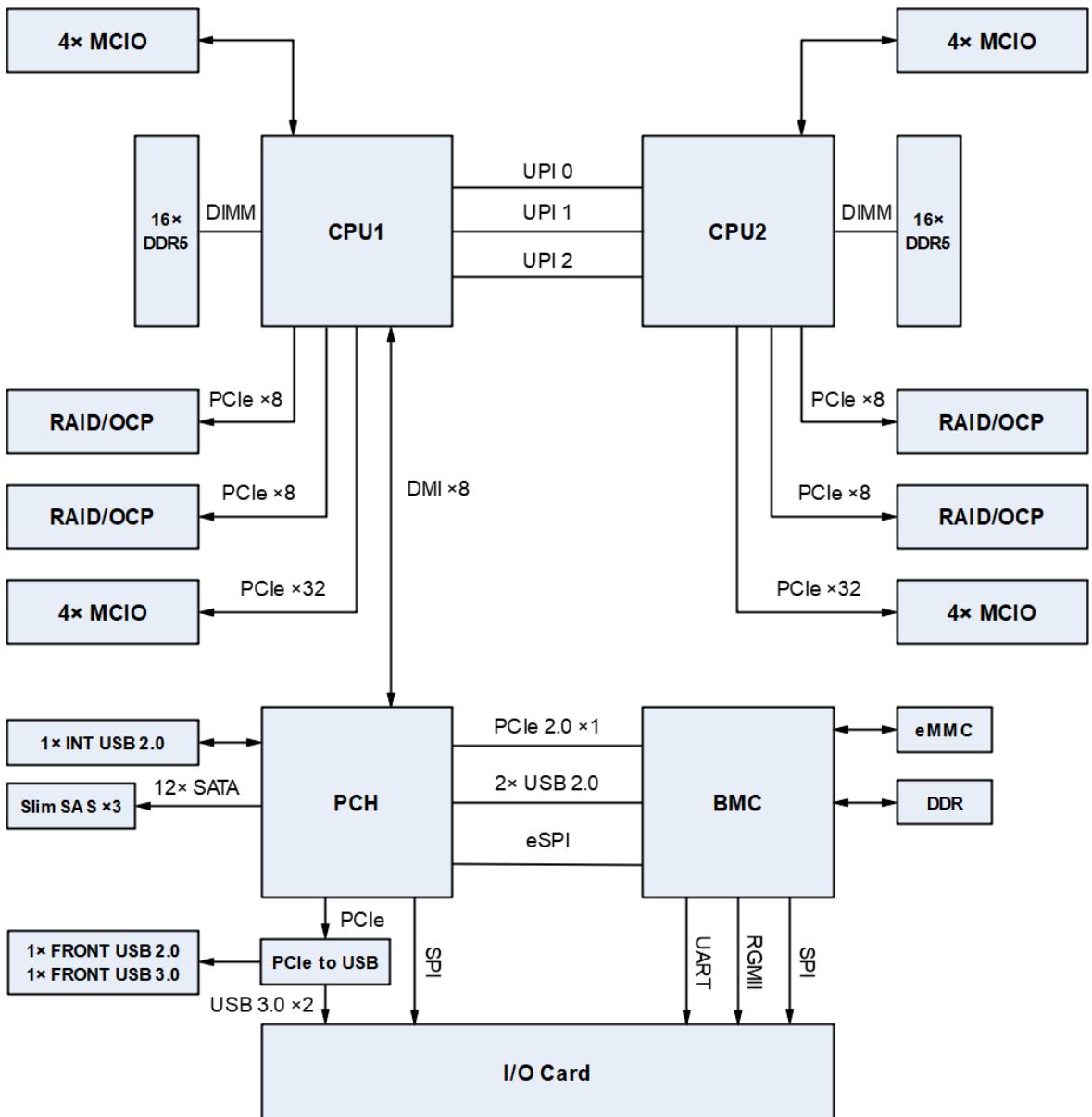
| No. | Component       | No. | Component                 |
|-----|-----------------|-----|---------------------------|
| 1   | Front hard disk | 2   | Front hard disk backplane |
| 3   | Chassis         | 4   | Mainboard                 |
| 5   | Fan unit        | 6   | Fan tray                  |
| 7   | Memory module   | 8   | GPU bracket               |

| No. | Component                   | No. | Component     |
|-----|-----------------------------|-----|---------------|
| 9   | PCIe switch board           | 10  | TPM card      |
| 11  | I/O card                    | 12  | Power adapter |
| 13  | Power module                | 14  | OCP card      |
| 15  | OCP adapter                 | 16  | GPU           |
| 17  | CPU                         | 18  | Heat sink     |
| 19  | RAID controller card module | 20  | Air duct      |

## 1.2 Logical Structure

### 1.2.1 Mainboard

Figure 1-2 shows the system modules of the NCS6742G N4 server and the logical relationships among these modules.

**Figure 1-2 Logical Structure**

For a description of the modules of the NCS6742G N4 server, refer to [Table 1-1](#).

**Table 1-1 Module Descriptions**

| Module | Description   |
|--------|---|
| CPU    | Used for processing information and running programs as the calculation and control core of the server. The NCS6742G N4 server supports a maximum of two CPUs, which are interconnected through three <b>UPI</b> links, with the maximum transmission rate of 20 GT/s per link. |
| DDR5   | Used for storing computational data in the CPUs and the data exchanged with external storage such as hard disks. The NCS6742G N4 server provides 32 DDR5 <b>DIMM</b> slots.   |

| Module   | Description   |
|----------|---|
| MCIO     | High-speed signal connector, which is connected to the hard disk backplane and switch board.  |
| RAID     | Hard disk <a href="#">RAID</a> controller, which protects storage device data and supports common RAID levels such as RAID 0, RAID 1, RAID 5, RAID 6, RAID 10, RAID 50 and RAID 60.                                 |
| OCP      | Used for expanding the network capacity of the server. The NCS6742G N4 server supports various standard OCP <a href="#">NIC</a> 3.0 cards.  |
| PCH      | Southbridge chipset on the mainboard of the server. <a href="#">SATA</a> , <a href="#">PCIe</a> , and <a href="#">USB</a> interfaces can be integrated into it. The NCS6742G N4 server uses the Emmitsburg chipset. |
| USB      | Exchanges data between the server and external devices. The NCS6742G N4 server provides one USB 2.0 interface and three USB 3.0 interfaces.   |
| SlimSAS  | High-speed signal connector, which is connected to the hard disk backplane and RAID adapter.  |
| SATA     | Hard disk interface specification. The NCS6742G N4 server provides twenty SATA 3.0 interfaces.  |
| BIOS     | Provides the most basic and direct hardware configuration and control for the server.   |
| BMC      | Used for upgrading server firmware and viewing device information when the server is not powered on.  |
| DDR      | Supports BMC operation.   |
| I/O Card | Provides one standard <a href="#">VGA</a> interface and two standard USB 3.0 interfaces.  |

## 1.2.2 Switch Boards

Through a [PCIe](#) switch board, the NCS6742G N4 server can provide standard PCIe slots to extend system functions.

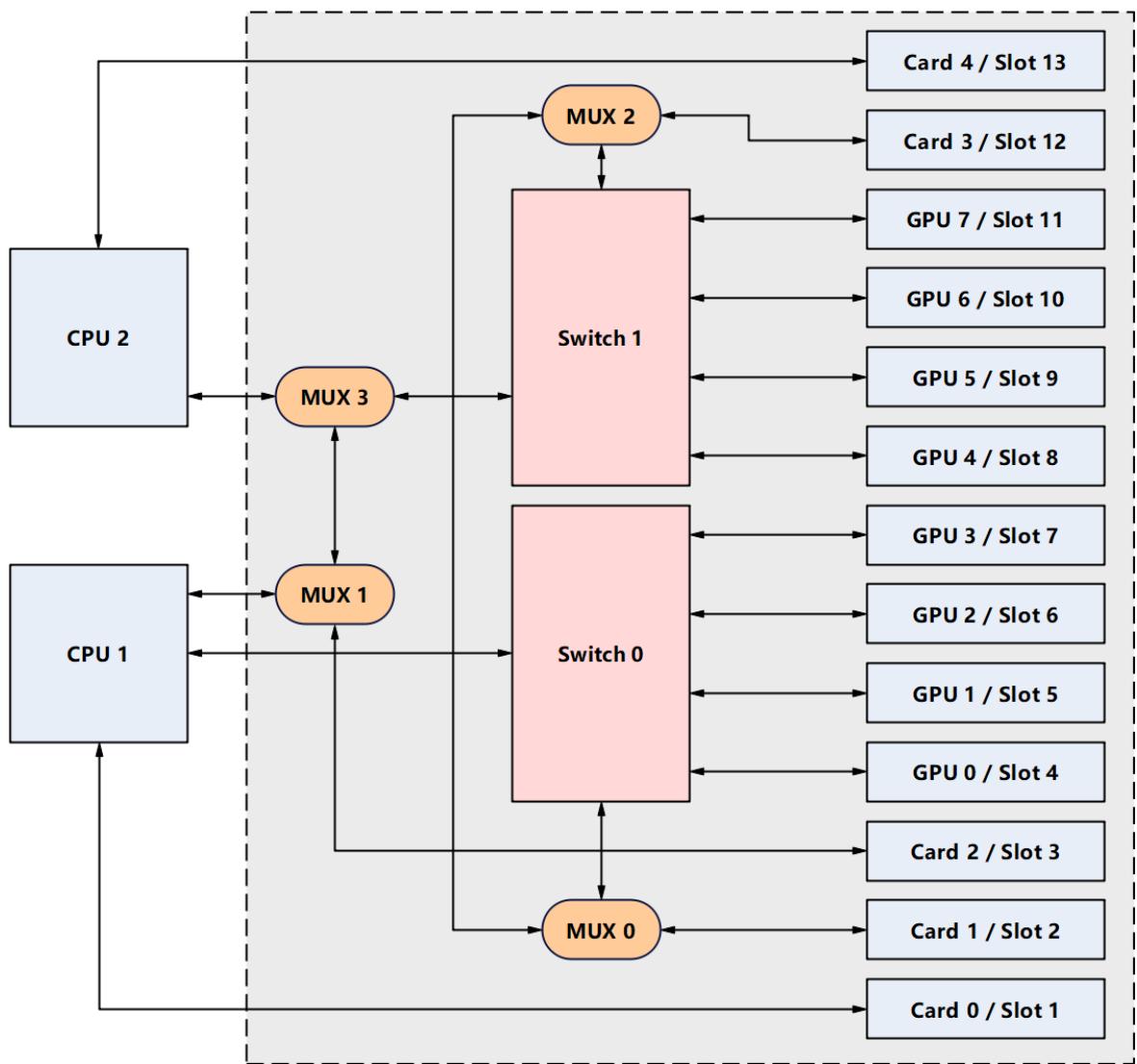
The NCS6742G N4 server supports the following types of switch boards:

- [1.2.2.1 13-Slot PCIe 4.0 Switch Board](#)
- [1.2.2.2 13-Slot PCIe 5.0 Switch Board](#)
- [1.2.2.3 21-Slot PCIe 4.0 Switch Board](#)
- [1.2.2.4 12-Slot PCIe 5.0 Pass-Through Board](#)

### 1.2.2.1 13-Slot PCIe 4.0 Switch Board

[Figure 1-3](#) shows the logical structure of a 13-slot [PCIe](#) 4.0 switch board.

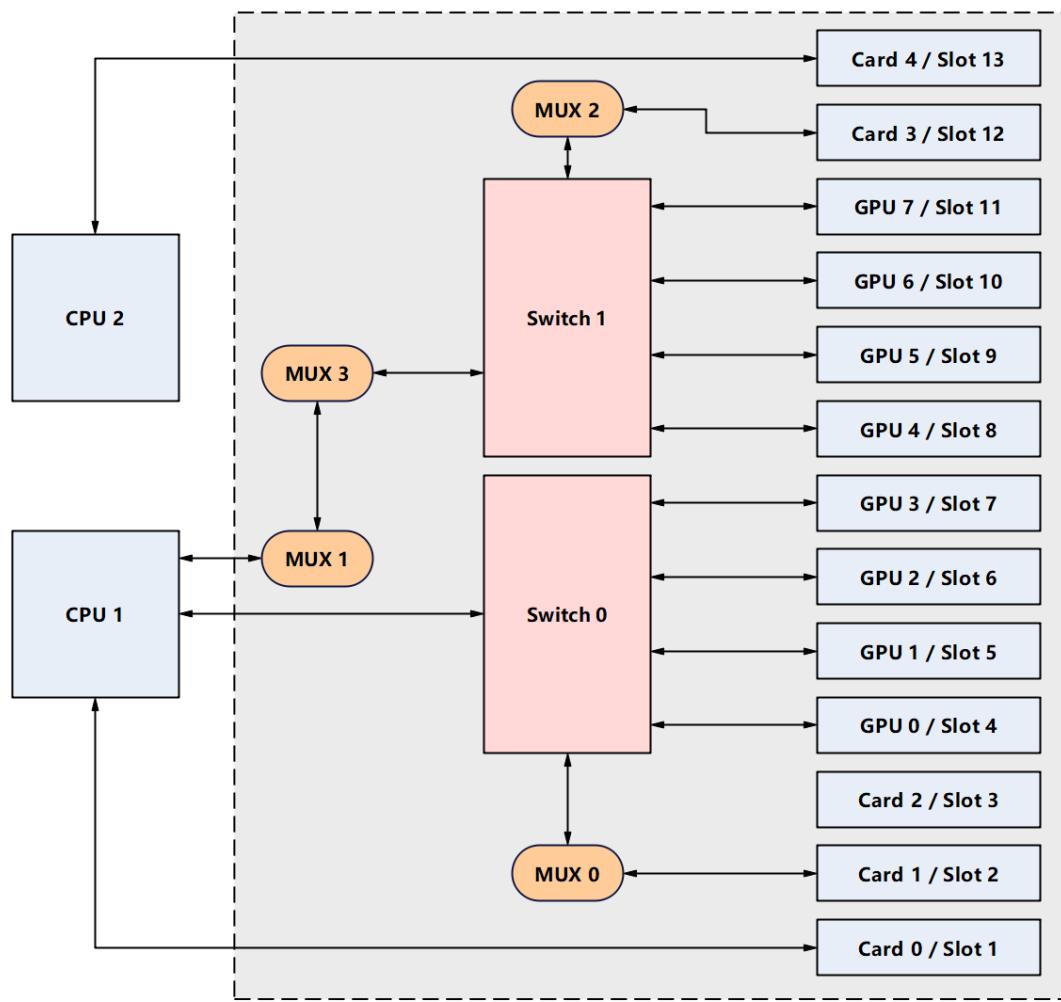
Figure 1-3 Logical Structure of a 13-Slot PCIe 4.0 Switch Board



The 13-slot PCIe 4.0 switch board supports working mode change in one click. The switch board operates in one of the following three modes:

- **Normal mode**

In normal mode, the server enables point-to-point communication between GPUs while guaranteeing sufficient I/O bandwidth between CPUs and GPUs. [Figure 1-4](#) shows the logical structure of the switch board in this mode.

**Figure 1-4 Logical Structure in Normal Mode**

For the relationships between connectors and the slots on the 13-slot PCIe 4.0 switch board in normal mode, refer to [Table 1-2](#).

**Table 1-2 Relationships Between Connectors and the Slots on the 13-Slot PCIe 4.0 Switch Board—Normal Mode**

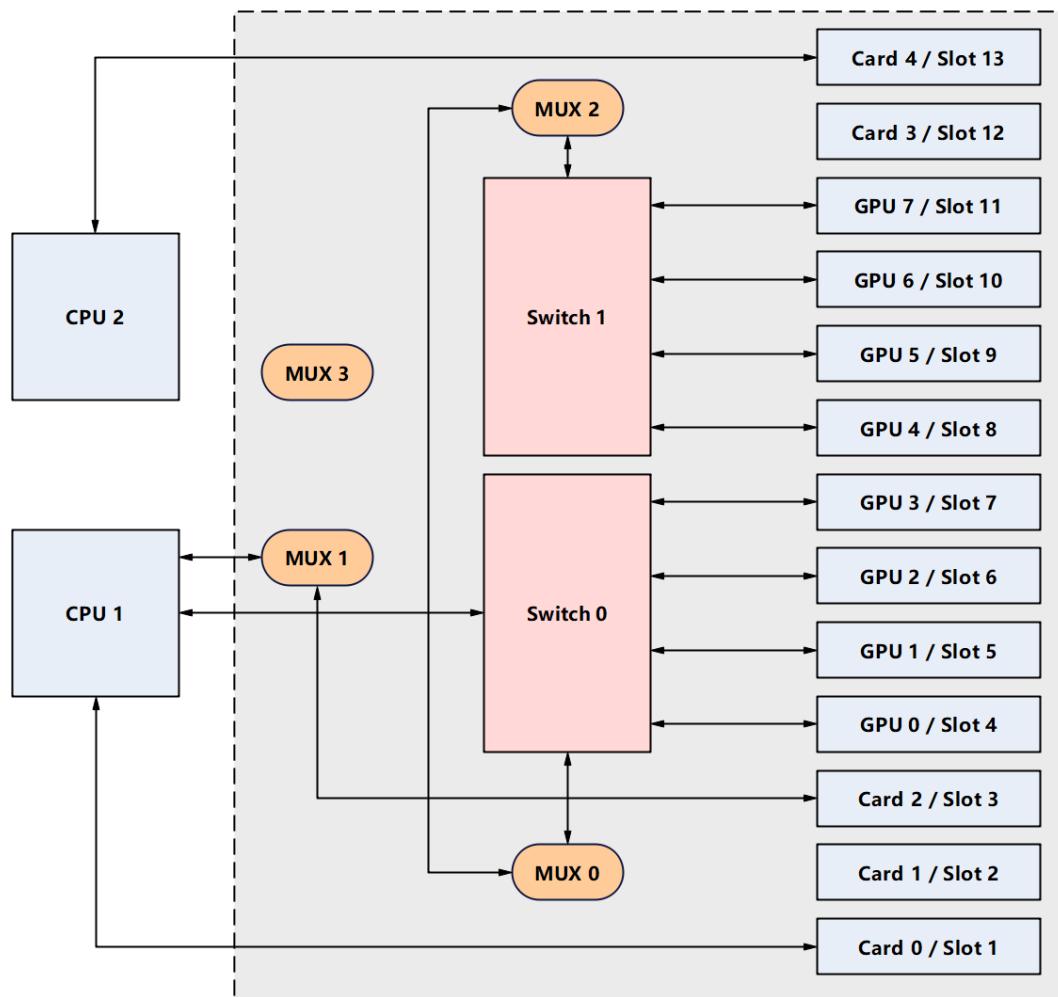
| Slot ID                            | Connector Position ID on the Switch Board | Connector Position ID on the Mainboard |
|------------------------------------|---|--|
| Slot 1                             | X5  | X14                                    |
|                                    | X7  | X48                                    |
| Switch 1:<br>Slot 8–Slot 12        | X2  | X42                                    |
|                                    | X4  | X46                                    |
| Switch 0:<br>Slot 2, Slot 4–Slot 7 | X1  | X41                                    |
|                                    | X3  | X44                                    |
| -                                  | X6  | X70                                    |

| Slot ID | Connector Position ID on the Switch Board | Connector Position ID on the Mainboard |
|---------|---|--|
| -       | X8  | X55                                    |
| Slot 13 | X4  | X53                                    |
|         | X10                                       | X54                                    |

- **Cascading mode**

In cascading mode, the server preferentially ensures point-to-point communication between GPUs, effectively reducing their communication delay. [Figure 1-5](#) shows the logical structure of the switch board in this mode.

[Figure 1-5 Logical Structure in Cascading Mode](#)



For the relationships between connectors and the slots on the 13-slot PCIe 4.0 switch board in cascading mode, refer to [Table 1-3](#).

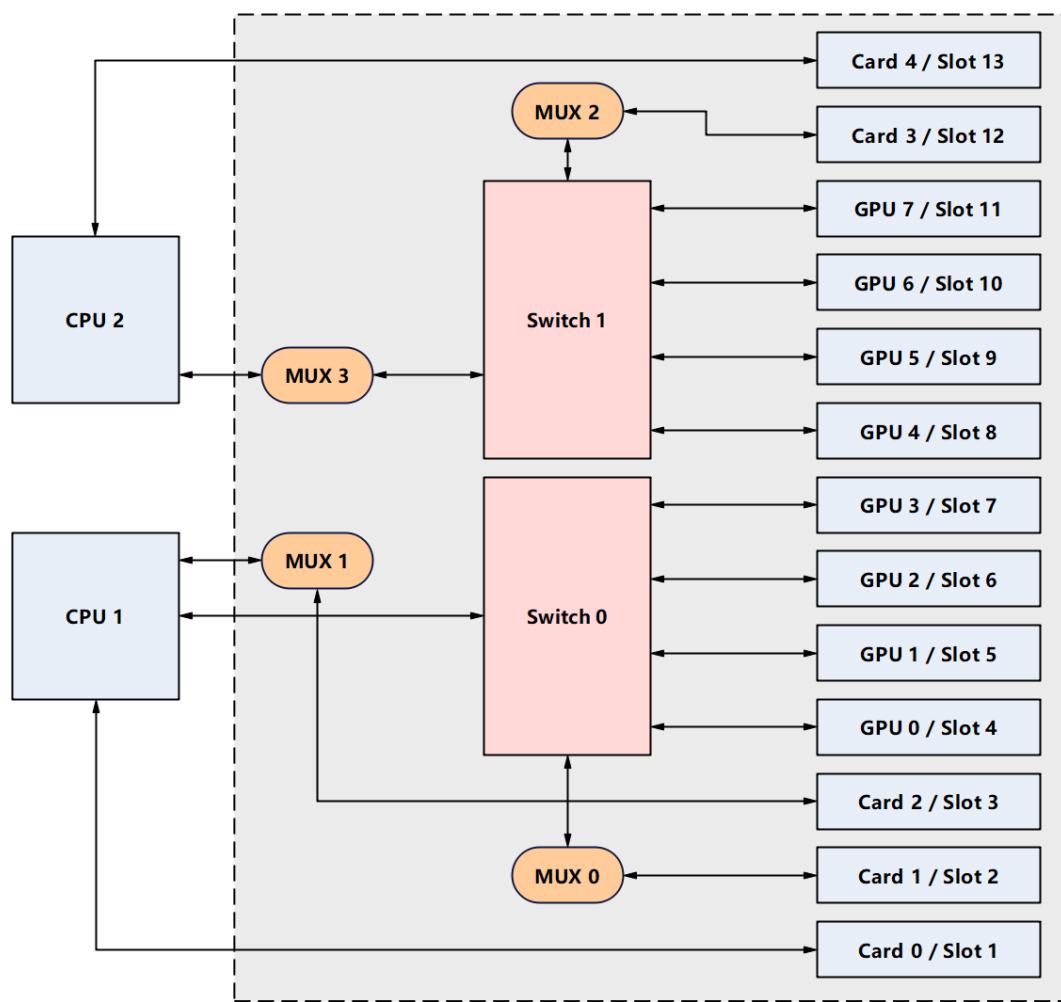
**Table 1-3 Relationships Between Connectors and the Slots on the 13-Slot PCIe 4.0 Switch Board—Cascading Mode**

| Slot ID                                  | Connector Position ID on the Switch Board | Connector Position ID on the Mainboard |
|--|---|--|
| Slot 1                                   | X5  | X14                                    |
|  | X7  | X48                                    |
| Switch 0 and Switch 1:<br>Slot 4–Slot 11 | X2  | X42                                    |
|  | X4  | X46                                    |
|  | X1  | X41                                    |
|  | X3  | X44                                    |
| Slot 3                                   | X6  | X70                                    |
|  | X8  | X55                                    |
| Slot 13                                  | X4  | X53                                    |
|  | X10                                       | X54                                    |

- **Balanced mode**

In balanced mode, the server provides better I/O bandwidth between CPUs and GPUs.

[Figure 1-6](#) shows the logical structure of the switch board in this mode.

**Figure 1-6 Logical Structure in Balanced Mode**

For the relationships between connectors and the slots on the 13-slot PCIe 4.0 switch board in balanced mode, refer to [Table 1-4](#).

**Table 1-4 Relationships Between Connectors and the Slots on the 13-Slot PCIe 4.0 Switch Board—Balanced Mode**

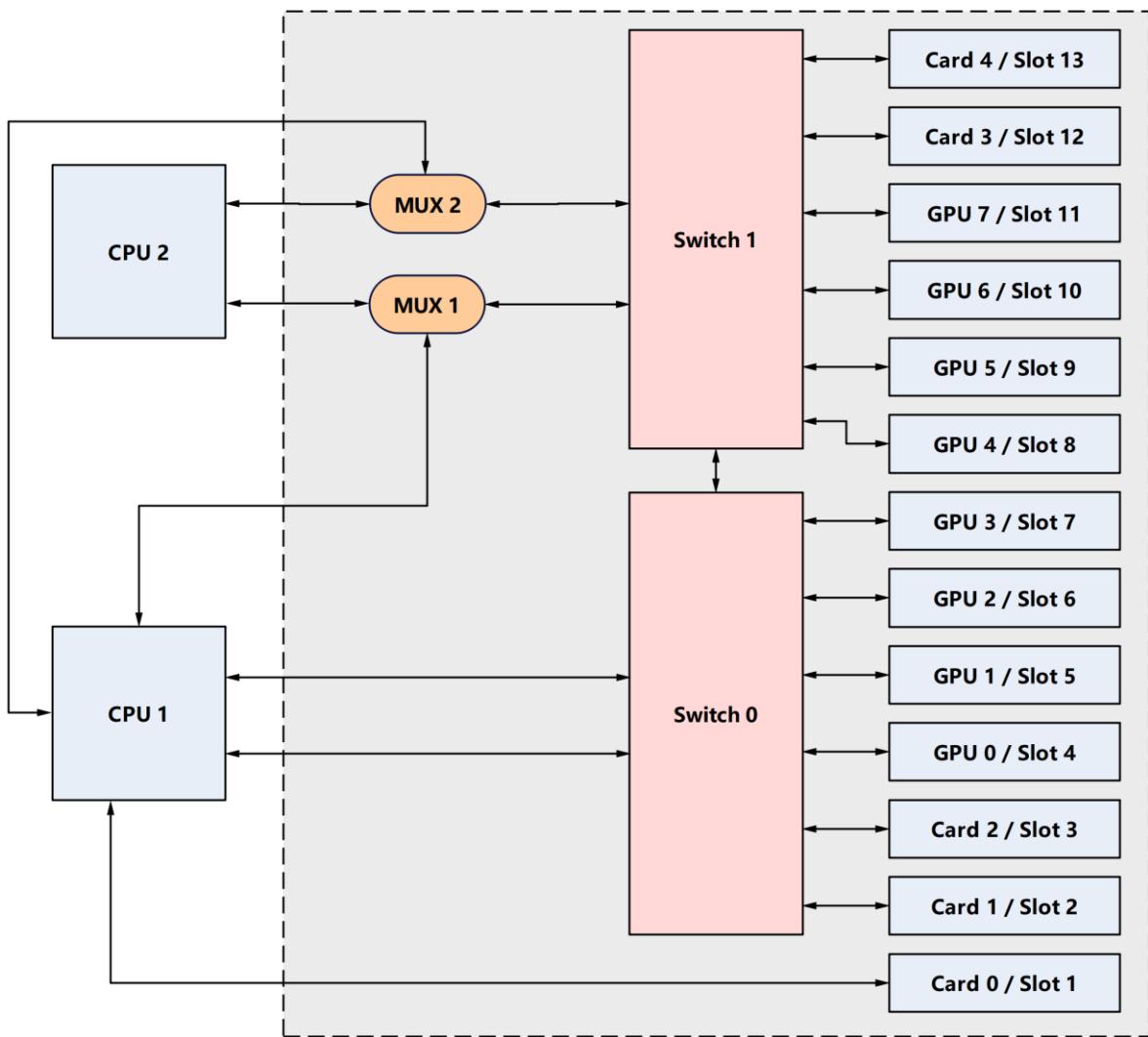
| Slot ID                            | Connector Position ID on the Switch Board | Connector Position ID on the Mainboard |
|------------------------------------|---|--|
| Slot 1                             | X5  | X14                                    |
|                                    | X7  | X48                                    |
| Slot 3                             | X2  | X42                                    |
|                                    | X4  | X46                                    |
| Switch 0:<br>Slot 2, Slot 4–Slot 7 | X1  | X41                                    |
|                                    | X3  | X44                                    |
| Switch 1:                          | X6  | X70                                    |

| Slot ID        | Connector Position ID on the Switch Board | Connector Position ID on the Mainboard |
|----------------|---|--|
| Slot 8–Slot 12 | X8  | X55                                    |
| Slot 13        | X4  | X53                                    |
|                | X10                                       | X54                                    |

### 1.2.2.2 13-Slot PCIe 5.0 Switch Board

Figure 1-7 shows the logical structure of a 13-slot PCIe 5.0 switch board.

**Figure 1-7 Logical Structure of a 13-Slot PCIe 5.0 Switch Board**

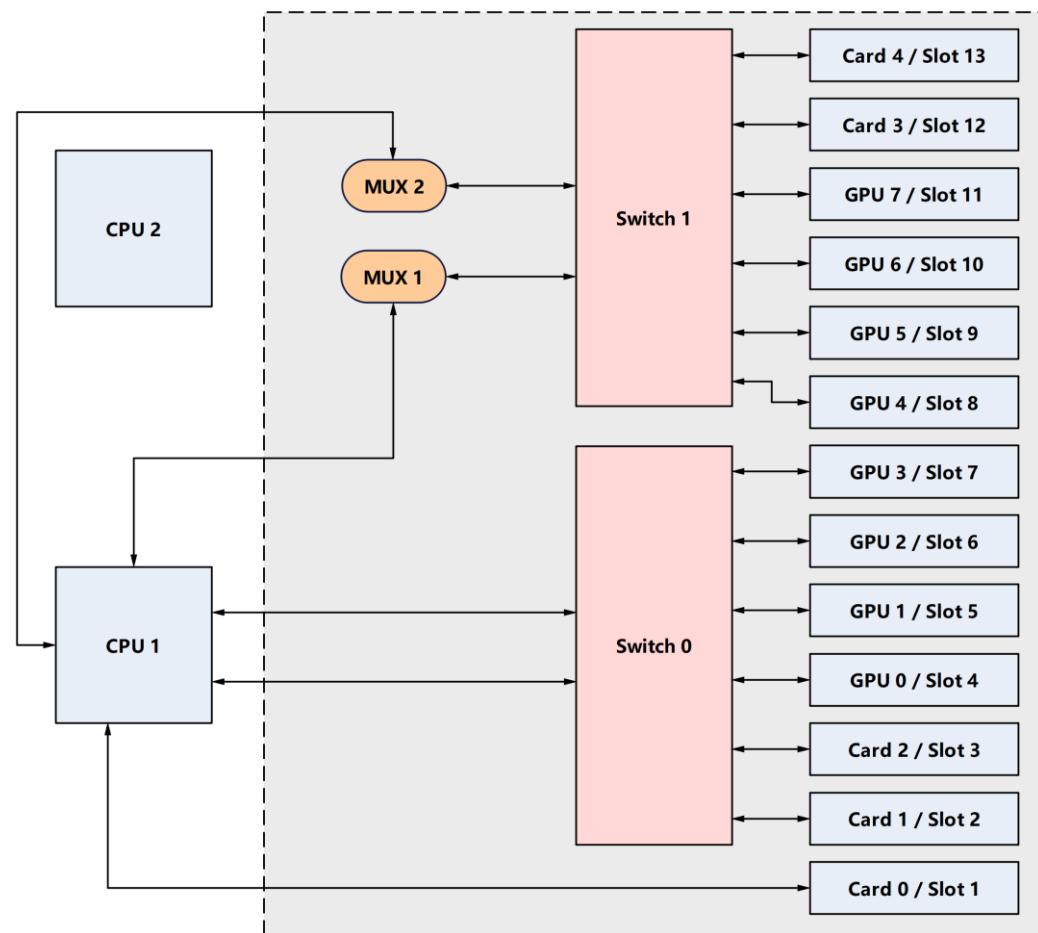


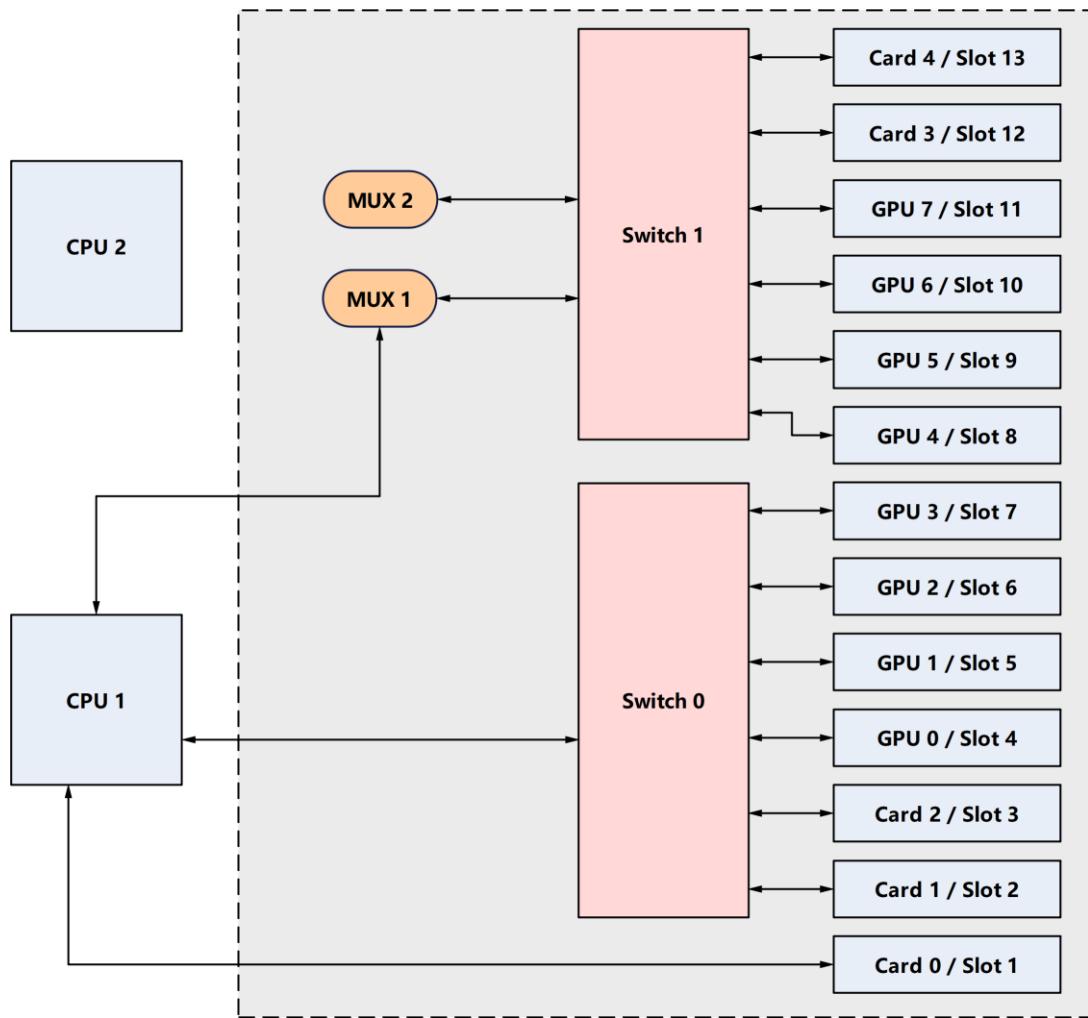
The 13-slot PCIe 5.0 switch board supports working mode change in one click. The switch board operates in one of the following three modes:

- **Normal mode**

In normal mode, the server enables point-to-point communication between GPUs while guaranteeing sufficient I/O bandwidth between CPUs and GPUs. Figure 1-8 and Figure 1-9 show the logical structure of the switch board in this mode.

**Figure 1-8 Logical Structure in Dual Uplink Normal Mode**



**Figure 1-9 Logical Structure in Single Uplink Normal Mode**

For the relationships between connectors and the slots on the 13-slot PCIe 5.0 switch board in normal mode, refer to [Table 1-5](#).

**Table 1-5 Relationships Between Connectors and the Slots on the 13-Slot PCIe 5.0 Switch Board—Normal Mode**

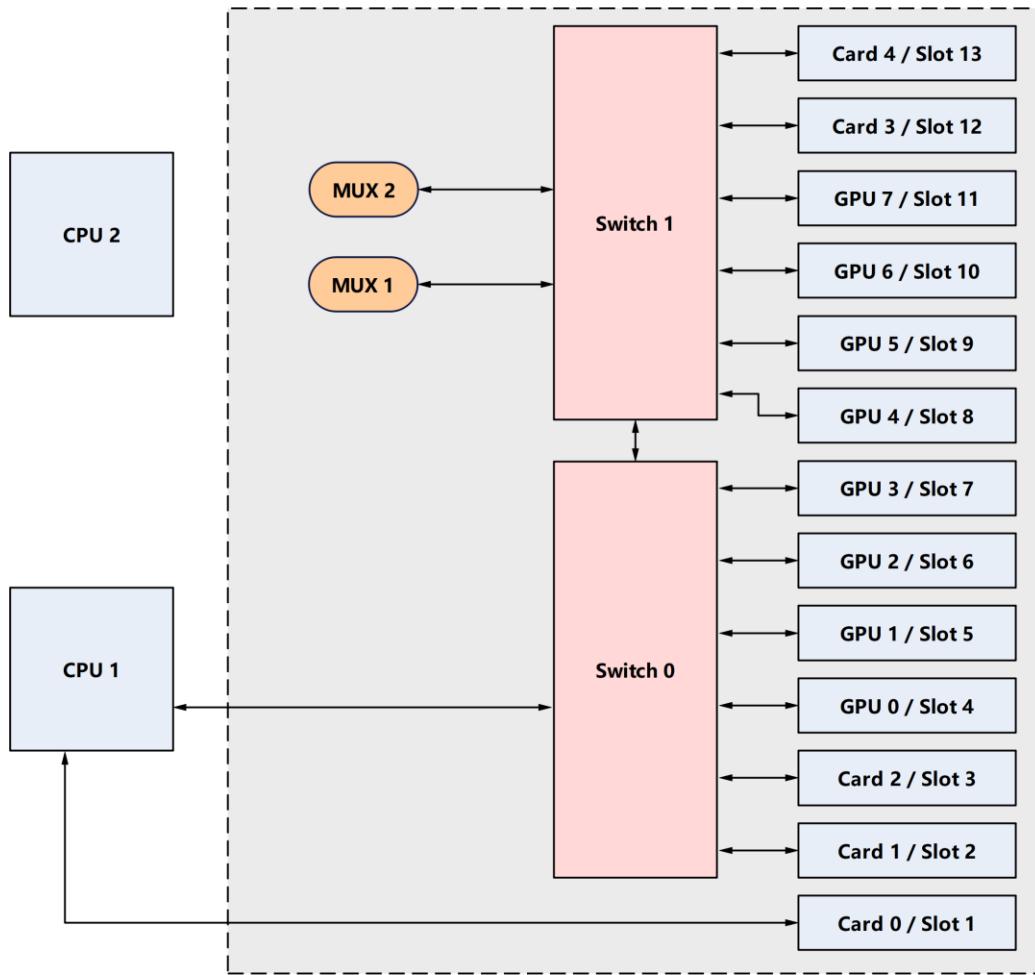
| Slot ID                     | Connector Position ID on the Switch Board | Connector Position ID on the Mainboard |
|-----------------------------|---|--|
| Slot 1                      | X5  | X14                                    |
|                             | X7  | X48                                    |
| Switch 1:<br>Slot 8–Slot 13 | X8  | X8                                     |
|                             | X6  | X47                                    |
| Switch 0:<br>Slot 2–Slot 7  | X2  | X42                                    |
|                             | X4  | X46                                    |
|                             | X1  | X41                                    |

| Slot ID                     | Connector Position ID on the Switch Board | Connector Position ID on the Mainboard |
|-----------------------------|---|--|
|                             | X3  | X44                                    |
| Switch 1:<br>Slot 8–Slot 13 | X54                                       | X56                                    |
|                             | X55                                       | X36                                    |
| -                           | X47                                       | X70                                    |
| -                           | X9  | X55                                    |
| -                           | X10                                       | X53                                    |
| -                           | X48                                       | X54                                    |

- **Cascading mode**

In cascading mode, the server preferentially ensures point-to-point communication between GPUs, effectively reducing their communication delay. [Figure 1-10](#) shows the logical structure of the switch board in this mode.

[Figure 1-10 Logical Structure in Cascading Mode](#)



For the relationships between connectors and the slots on the 13-slot PCIe 5.0 switch board in cascading mode, refer to [Table 1-6](#).

**Table 1-6 Relationships Between Connectors and the Slots on the 13-Slot PCIe 5.0 Switch Board—Cascading Mode**

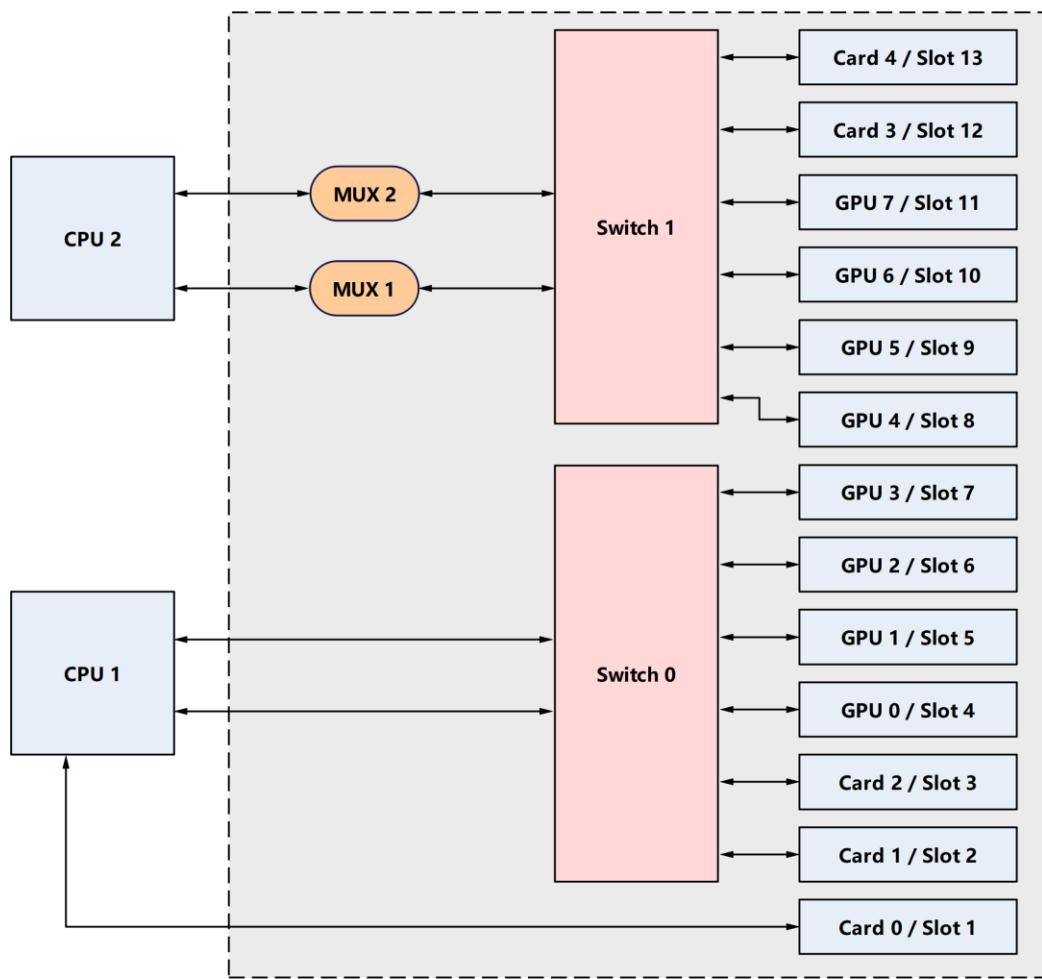
| Slot ID                                  | Connector Position ID on the Switch Board | Connector Position ID on the Mainboard |
|--|---|--|
| Slot 1                                   | X5  | X14                                    |
|  | X7  | X48                                    |
| -  | X8  | X8                                     |
| -  | X6  | X47                                    |
| Switch 0 and Switch 1:<br>Slot 2–Slot 13 | X2  | X42                                    |
|  | X4  | X46                                    |
| -  | X1  | X41                                    |
| -  | X3  | X44                                    |
| -  | X54                                       | X56                                    |
| -  | X55                                       | X36                                    |
| -  | X47                                       | X70                                    |
| -  | X9  | X55                                    |
| -  | X10                                       | X53                                    |
| -  | X48                                       | X54                                    |

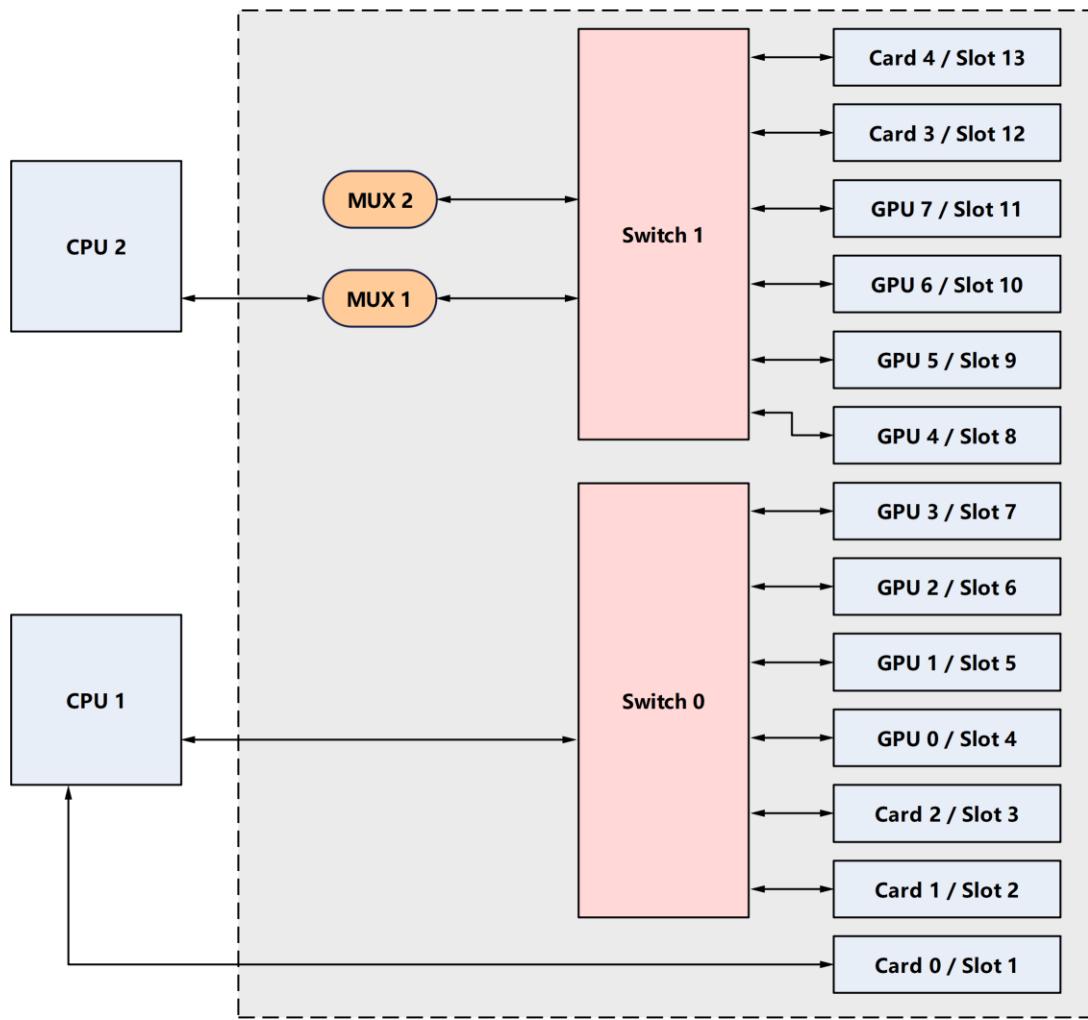
- Balanced mode

In balanced mode, the server provides better I/O bandwidth between CPUs and GPUs.

[Figure 1-11](#) and [Figure 1-12](#) show the logical structure of the switch board in this mode.

Figure 1-11 Logical Structure in Dual Uplink Balanced Mode



**Figure 1-12 Logical Structure in Single Uplink Balanced Mode**

For the relationships between connectors and the slots on the 13-slot PCIe 5.0 switch board in balanced mode, refer to [Table 1-7](#).

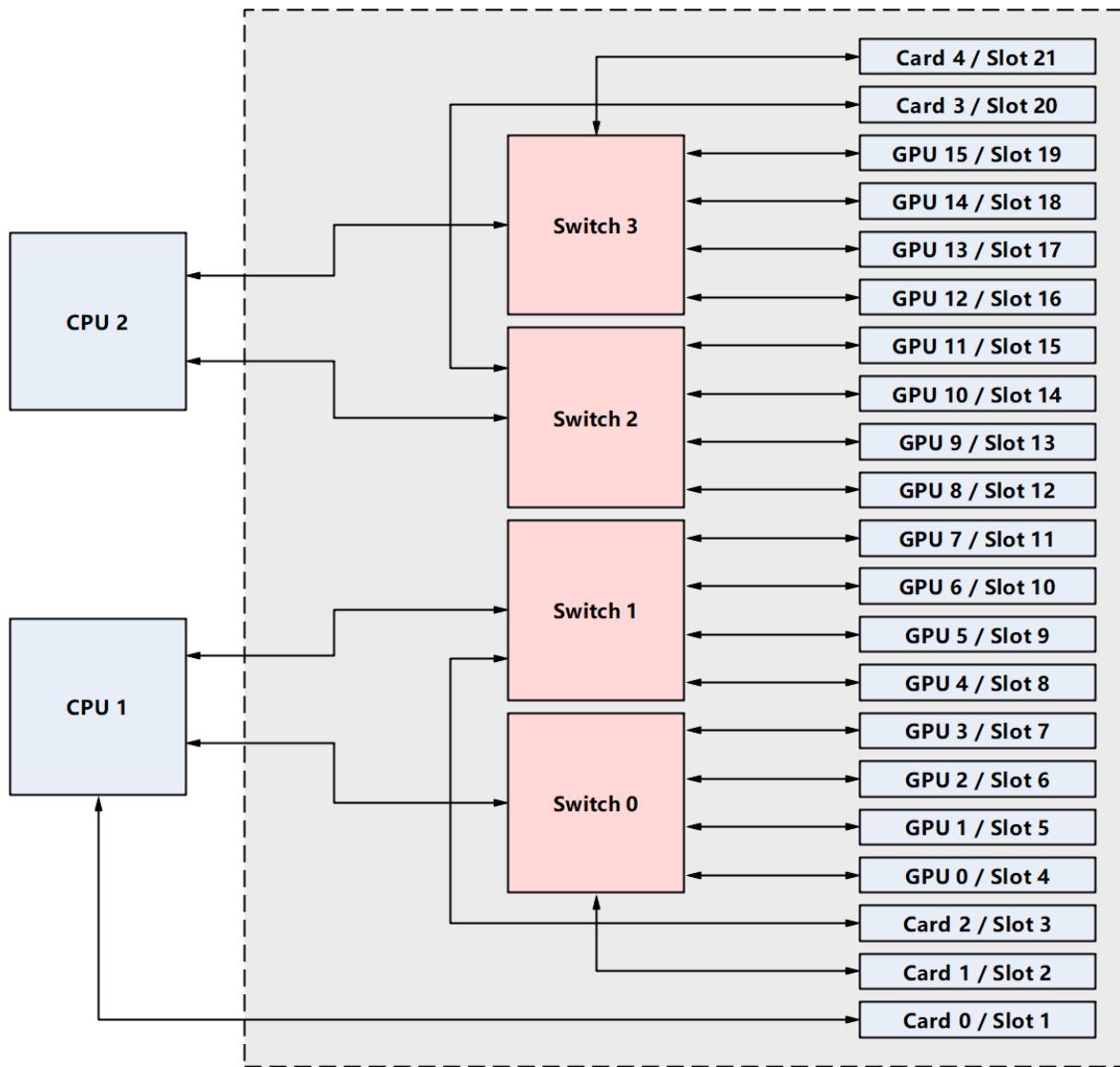
**Table 1-7 Relationships Between Connectors and the Slots on the 13-Slot PCIe 5.0 Switch Board—Balanced Mode**

| Slot ID                    | Connector Position ID on the Switch Board | Connector Position ID on the Mainboard |
|----------------------------|---|--|
| Slot 1                     | X5  | X14                                    |
|                            | X7  | X48                                    |
| -                          | X8  | X8                                     |
| -                          | X6  | X47                                    |
| Switch 0:<br>Slot 2–Slot 7 | X2  | X42                                    |
|                            | X4  | X46                                    |
|                            | X1  | X41                                    |

| Slot ID                     | Connector Position ID on the Switch Board | Connector Position ID on the Mainboard |
|-----------------------------|---|--|
|                             | X3  | X44                                    |
| -                           | X54                                       | X56                                    |
| -                           | X55                                       | X36                                    |
| Switch 1:<br>Slot 8–Slot 13 | X47                                       | X70                                    |
|                             | X9  | X55                                    |
|                             | X10                                       | X53                                    |
|                             | X48                                       | X54                                    |

### 1.2.2.3 21-Slot PCIe 4.0 Switch Board

[Figure 1-13](#) shows the logical structure of a 21-slot PCIe 4.0 switch board.

**Figure 1-13 Logical Structure of a 21-Slot PCIe 4.0 Switch Board**

For the relationships between connectors and the slots on the 21-slot PCIe 4.0 switch board, refer to [Table 1-8](#).

**Table 1-8 Relationships Between Connectors and the Slots on the 21-Slot PCIe 4.0 Switch Board**

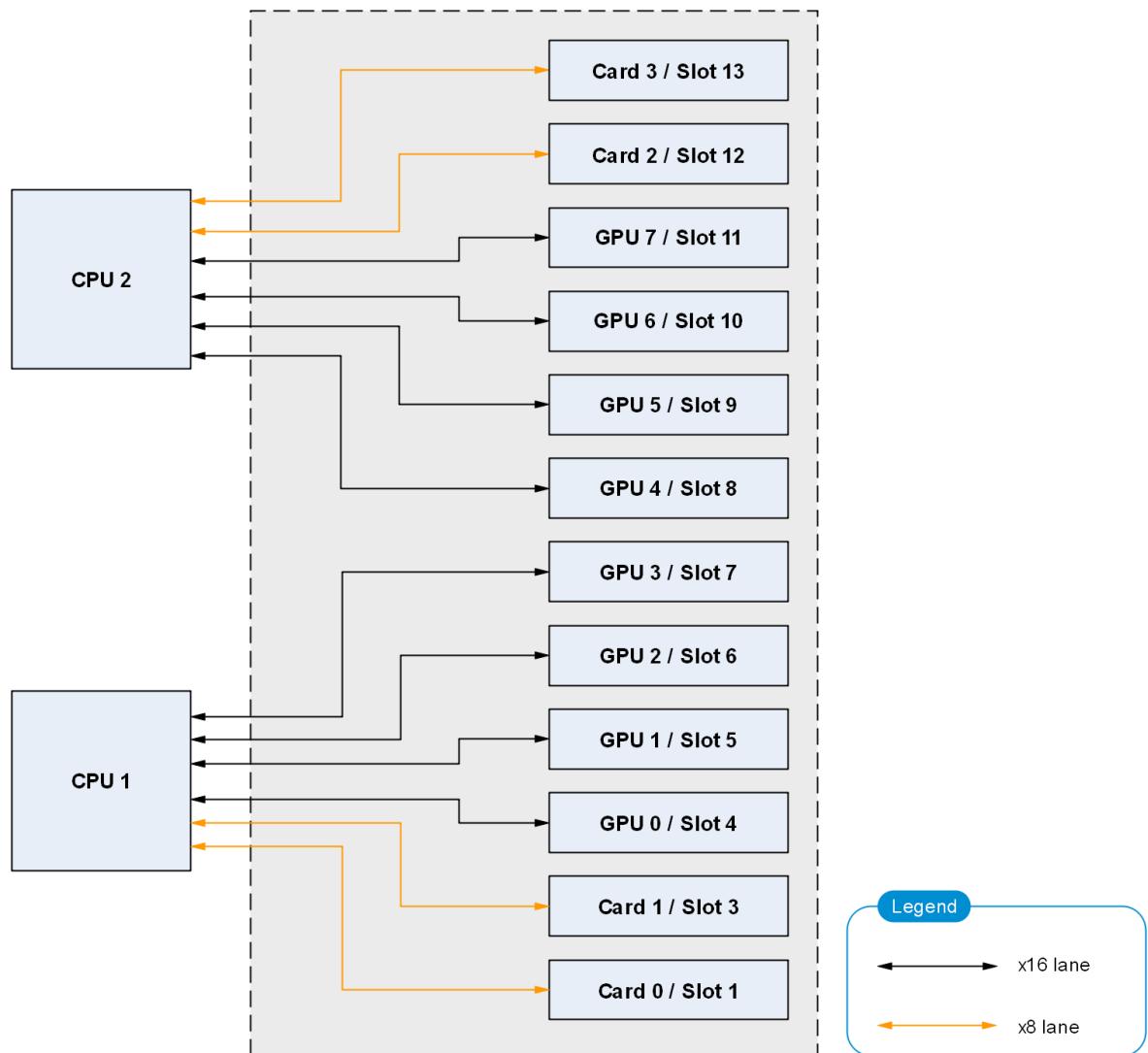
| Slot ID                            | Connector Position ID on the Switch Board | Connector Position ID on the Mainboard |
|------------------------------------|---|--|
| Slot 1                             | X73                                       | X14                                    |
|                                    | X7  | X48                                    |
| Switch 0:<br>Slot 2, Slot 4–Slot 7 | X2  | X42                                    |
|                                    | X4  | X46                                    |
| Switch 1:                          | X1  | X41                                    |

| Slot ID                               | Connector Position ID on the Switch Board | Connector Position ID on the Mainboard |
|---------------------------------------|---|--|
| Slot 3, Slot 8–Slot 11                | X3  | X44                                    |
| Switch 2:<br>Slot 12–Slot 15, Slot 20 | X6  | X70                                    |
|                                       | X8  | X55                                    |
| Switch 3:<br>Slot 16–Slot 19, Slot 21 | X9  | X53                                    |
|                                       | X10                                       | X54                                    |

#### 1.2.2.4 12-Slot PCIe 5.0 Pass-Through Board

Figure 1-14 shows the logical structure of a 12-slot PCIe 5.0 pass-through board.

**Figure 1-14 Logical Structure of a 12-Slot PCIe 5.0 Pass-Through Board**



For the relationships between connectors and the slots on the 12-slot PCIe 5.0 pass-through board, refer to [Table 1-9](#).

**Table 1-9 Relationships Between Connectors and the Slots on the 12-Slot PCIe 5.0 Pass-Through Board**

| Slot ID | Connector Position ID on the Pass-Through Board | Connector Position ID on the Mainboard |
|---------|---|--|
| Slot 1  | X7  | X14                                    |
|         | X5  | X48                                    |
| Slot 3  | X6  | X48                                    |
| Slot 4  | X8  | X8                                     |
|         | X10   | X47                                    |
| Slot 5  | X9  | X42                                    |
|         | X11   | X46                                    |
| Slot 6  | X14   | X41                                    |
|         | X12   | X44                                    |
| Slot 7  | X13   | X56                                    |
|         | X15   | X36                                    |
| Slot 8  | X17   | X58                                    |
|         | X19   | X28                                    |
| Slot 9  | X16   | X70                                    |
|         | X18   | X55                                    |
| Slot 10 | X20   | X53                                    |
|         | X22   | X54                                    |
| Slot 11 | X21   | X13                                    |
|         | X23   | X18                                    |
| Slot 12 | X25   | X50                                    |
| Slot 13 | X24   | X49                                    |
|         | X26   | X50                                    |

# Chapter 2

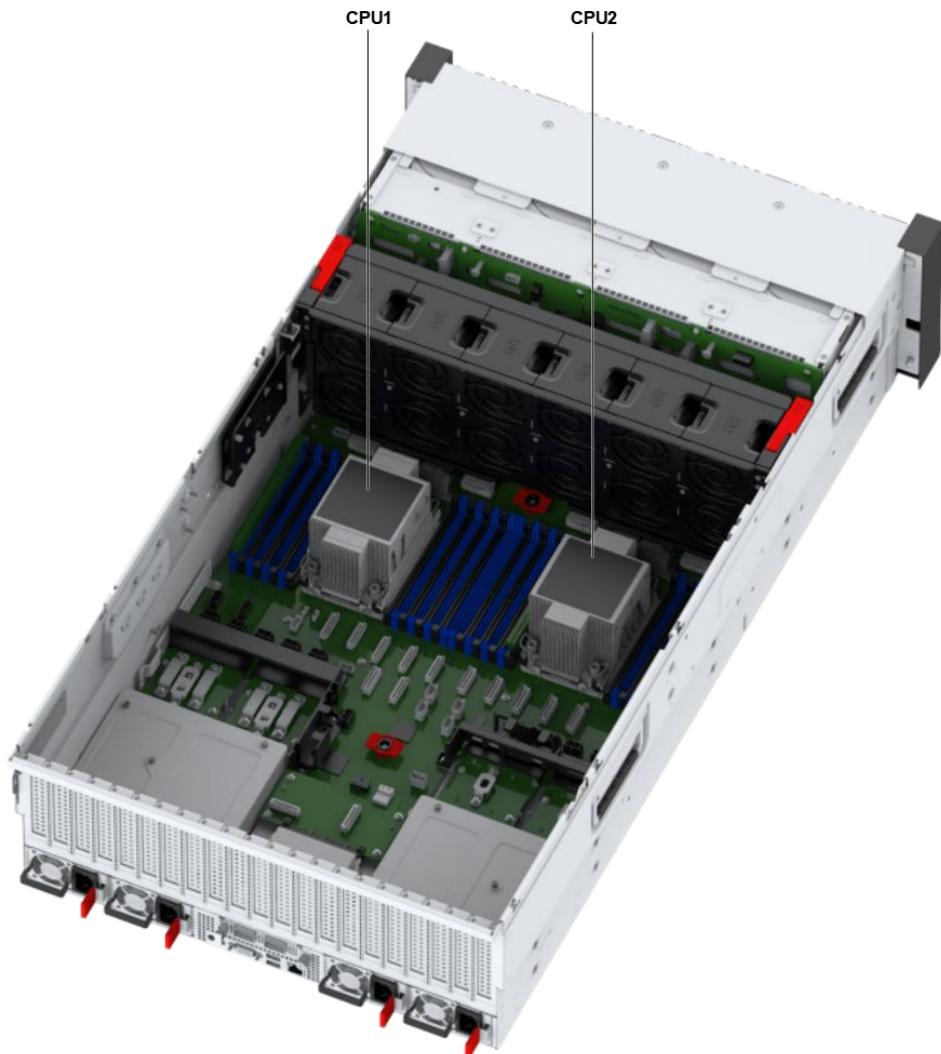
# CPU

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The NCS6742G N4 server uses a dual-CPU design, supporting <sup>®</sup> Xeon <sup>®</sup> Scalable processors ( Intel Sapphire Rapids/Emerald Rapids).

[Figure 2-1](#) shows the positions of CPUs in the NCS6742G N4.

**Figure 2-1 Positions of CPUs**



The following CPU configuration in [Table 2-1](#) is recommended for the NCS6742G N4 server to maximize system performance and functions.

**Table 2-1 Recommended CPU Configuration**

| Number of CPUs | CPU1 | CPU2 |
|----------------|------|------|
| Two            | √    | √    |
| One            | √    | -    |

- "√" indicates to install a CPU in the slot.
- "-" indicates not to install a CPU in the slot.

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### Notice

The CPUs installed in a server must be of the same model.

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# Chapter 3

## DIMM

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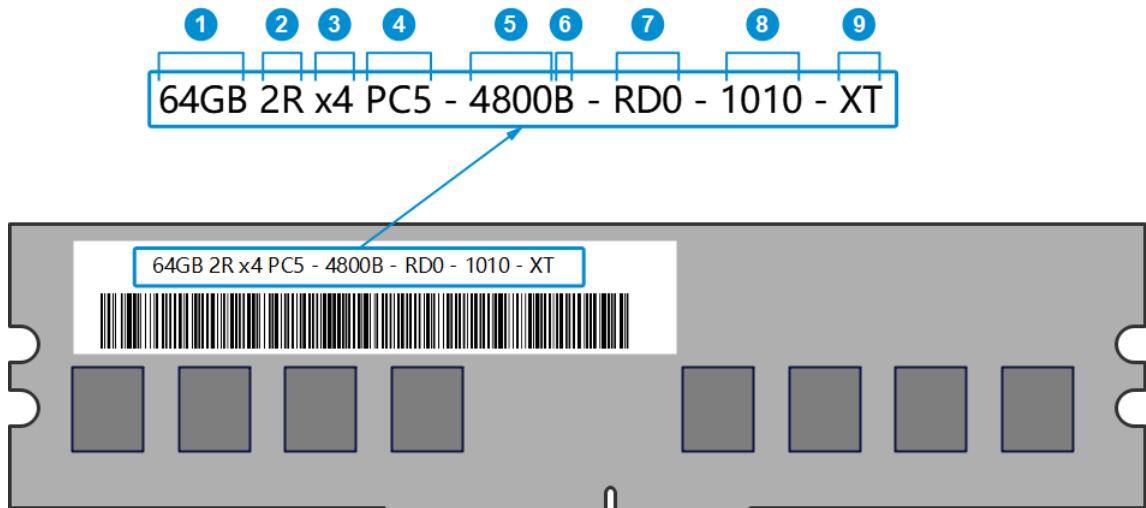
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### 3.1 DIMM Label

A **DIMM** label specifies the attributes of a DIMM. Figure 3-1 shows a typical DIMM label.

**Figure 3-1 DIMM Label**



For a description of the DIMM label, refer to [Table 3-1](#).

**Table 3-1 DIMM Label Descriptions**

| No. | Attribute | Description   |
|-----|-----------|---|
| 1   | Capacity  | <ul style="list-style-type: none"><li>• 16 GB</li><li>• 32 GB</li></ul> |

| No. | Attribute                 | Description  |
|-----|---------------------------|--|
|     |                           | <ul style="list-style-type: none"> <li>● 64 GB</li> <li>● 128 GB</li> <li>● 256 GB</li> </ul>  |
| 2   | Rank                      | <ul style="list-style-type: none"> <li>● 1R = single-ranked</li> <li>● 2R = dual-ranked</li> <li>● 4R = quad-ranked</li> <li>● 8R = octo-ranked</li> </ul>                       |
| 3   | DRAM data-bus width       | <ul style="list-style-type: none"> <li>● x4 = 4 bits</li> <li>● x8 = 8 bits</li> </ul>   |
| 4   | DIMM connector type       | PC5 = DDR5   |
| 5   | Maximum memory speed      | 4800 MT/s  |
| 6   | CAS latency (CL-nRCD-nRP) | <ul style="list-style-type: none"> <li>● AN = 34-34-34</li> <li>● B = 40-39-39</li> <li>● BN = 40-40-40</li> <li>● C = 42-42-42</li> </ul>                                       |
| 7   | DIMM type                 | RD0: RDIMM D0  |
| 8   | SPD version               | <ul style="list-style-type: none"> <li>● First 10: SPD revision level (basic section)</li> <li>● Last 10: SPD revision level (specific section, namely bytes 192–447)</li> </ul> |
| 9   | Temperature grade         | <ul style="list-style-type: none"> <li>● XT (Extended Temperature grade): 0#–95°C</li> <li>● NT (Normal Temperature grade): 0#–85°C</li> </ul>                                   |

## 3.2 DIMM Compatibility Rules

DDR5 is a computer memory specification. Compared with DDR4 memory, DDR5 memory has higher speed and bandwidth, lower power consumption, and higher stability and reliability.

The following compatibility rules apply when you install DDR5 DIMMs:

- The NCS6742G N4 server must use DDR5 DIMMs of the same model. The memory speed is the lower one of the following:
  - ➔ Maximum memory speed supported by the [CPUs](#).
  - ➔ Maximum operating speed of the DIMMs.
- Mix of different types ([RDIMM](#) and RDIMM-3DS) and specifications (capacity, data-bus width, rank and height) of DDR5 DIMMs is not allowed.
- The total memory capacity equals the sum of all DDR5 DIMM capacities.
- The maximum number of DIMMs depends on the types of DIMMs and number of ranks.

For parameter descriptions of the DDR5 DIMMs supported by the server, refer to [Table 3-2](#).

**Table 3-2 DDR5 DIMM Parameter Descriptions**

| Item   | Value             |   |       |           |           |
|--|-------------------|---|-------|-----------|-----------|
| Capacity (GB) of a single DDR5 DIMM                    | 16                | 32  | 64    | 128       | 256       |
| Type   | RDIMM             | RDIMM   | RDIMM | RDIMM-3DS | RDIMM-3DS |
| Rated memory speed (MT/s)                              | 5600              | 5600  | 5600  | 5600      | 5600      |
| Operating voltage (V)                                  | 1.1               | 1.1   | 1.1   | 1.1       | 1.1       |
| Maximum number of DDR5 DIMMs <sup>1</sup>              | 32                | 32  | 32    | 32        | 32        |
| Maximum total capacity (GB) of DDR5 DIMMs <sup>2</sup> | 512               | 1024  | 2048  | 4096      | 8192      |
| Maximum operating speed (MT/s)                         | 1DPC <sup>3</sup> | <ul style="list-style-type: none"> <li>Sapphire Rapids processor: 4800</li> <li>Emerald Rapids processor: 5600</li> </ul> |       |           |           |
|  | 2DPC              | 4400  | 4400  | 4400      | 4400      |

1. By default, the server with two CPUs supports a maximum of 32 DDR5 DIMMs. If the server is configured with only one CPU, the maximum number of DDR5 DIMMs supported is 16.
2. The maximum total capacity of DDR5 DIMMs depends on the types of CPUs and is the value in full memory configuration.
3. DIMM Per Channel (DPC) indicates the number of DIMMs installed in each memory channel.

### 3.3 DIMM Installation Guidelines

The general guidelines on installing DDR5 DIMMs are as follows:

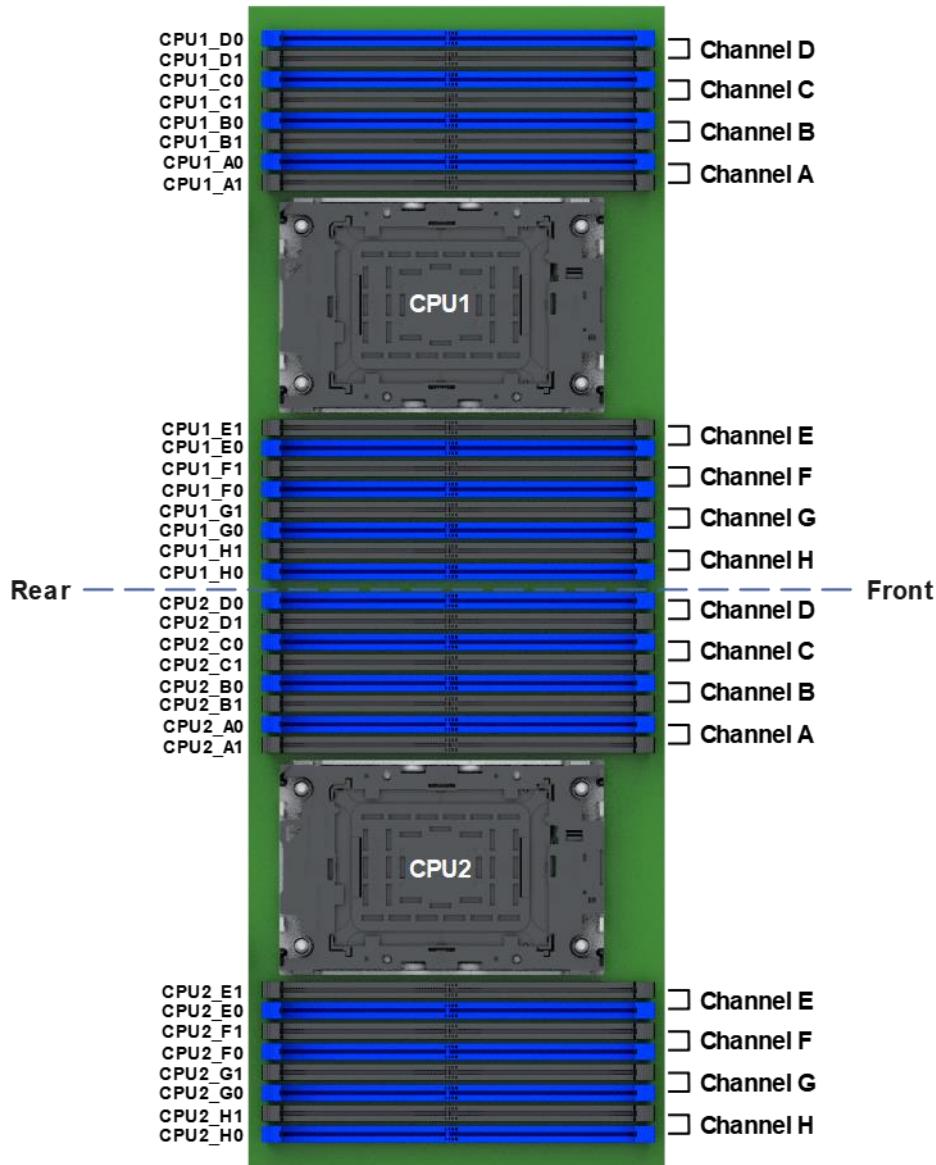
- For an SPR CPU (excluding HBM CPUs), at least one DDR5 DIMM needs to be configured. For an SPR HBM CPU, DDR5 DIMMs are optional.
- All the configured memory modules must be DDR5 RDIMMs.
- All the configured memory modules must have the same number of ranks.

### 3.4 DIMM Slot Positions

Each CPU in the NCS6742G N4 server provides eight memory channels, and each memory channel consists of two DIMM slots.

Therefore, the NCS6742G N4 server provides a maximum of 32 DDR5 DIMMs, with the highest rate up to 5600 MT/s.

Figure 3-2 shows the memory channels and DIMM slots of the NCS6742G N4 server.

**Figure 3-2 DIMM Slots**

- Front indicates the server front view.
- Rear indicates the server rear view.

For the relationships among the CPUs, memory channels, and DIMM slots of the NCS6742G N4 server, refer to [Table 3-3](#).

**Table 3-3 Relationships Among CPUs, Memory Channels and DIMM Slots**

| CPU  | Memory Channel | DIMM Slot | CPU  | Memory Channel | DIMM Slot |
|------|----------------|-----------|------|----------------|-----------|
| CPU1 | A              | CPU1_A0   | CPU2 | A              | CPU2_A0   |
|      |                | CPU1_A1   |      |                | CPU2_A1   |
|      | B              | CPU1_B0   |      | B              | CPU2_B0   |

| CPU | Memory Channel | DIMM Slot | CPU | Memory Channel | DIMM Slot |
|-----|----------------|-----------|-----|----------------|-----------|
|     | C              | CPU1_B1   |     | C              | CPU2_B1   |
|     |                | CPU1_C0   |     |                | CPU2_C0   |
|     |                | CPU1_C1   |     |                | CPU2_C1   |
|     | D              | CPU1_D0   |     | D              | CPU2_D0   |
|     |                | CPU1_D1   |     |                | CPU2_D1   |
|     | E              | CPU1_E0   |     | E              | CPU2_E0   |
|     |                | CPU1_E1   |     |                | CPU2_E1   |
|     | F              | CPU1_F0   |     | F              | CPU2_F0   |
|     |                | CPU1_F1   |     |                | CPU2_F1   |
|     | G              | CPU1_G0   |     | G              | CPU2_G0   |
|     |                | CPU1_G1   |     |                | CPU2_G1   |
|     | H              | CPU1_H0   |     | H              | CPU2_H0   |
|     |                | CPU1_H1   |     |                | CPU2_H1   |

### 3.5 Recommended DIMM Configuration



#### Notice

This section recommends the number and layout of **DIMMs** in different scenarios, which help to maximize memory performance.

#### Recommended DIMM Configuration (One CPU)

Figure 3-3 shows the configuration of DIMMs when one **CPU** (CPU1) is configured for the NCS6742G N4 server.

**Figure 3-3 Recommended DIMM Configuration (One CPU)**

| DDR5 Qty | D | CPU1_D0 | CPU1_D1 | CPU1_C0 | CPU1_C1 | CPU1_B0 | CPU1_B1 | A | CPU1_A0 | CPU1_A1 |   |   |   |   |
|----------|---|---------|---------|---------|---------|---------|---------|---|---------|---------|---|---|---|---|
|          |   |         |         |         |         |         |         |   |         |         | E | F | G | H |
| 1        | - | -       | -       | -       | -       | -       | -       | - | ✓       | -       | - | - | - | - |
| 2        | - | -       | -       | -       | -       | -       | -       | - | ✓       | -       | - | - | - | - |
| 4        | - | -       | ✓       | -       | -       | -       | -       | - | ✓       | -       | - | ✓ | - | - |
| 6        | ✓ | -       | ✓       | -       | -       | -       | -       | - | ✓       | -       | - | ✓ | - | - |
| 8        | ✓ | -       | ✓       | -       | ✓       | -       | ✓       | - | ✓       | -       | - | ✓ | - | ✓ |
| 12       | ✓ | -       | ✓       | ✓       | ✓       | -       | ✓       | ✓ | ✓       | ✓       | ✓ | ✓ | - | ✓ |
| 16       | ✓ | ✓       | ✓       | ✓       | ✓       | ✓       | ✓       | ✓ | ✓       | ✓       | ✓ | ✓ | ✓ | ✓ |

- "-✓" indicates to install a DIMM.
- "-" indicates not to install a DIMM.

### Recommended DIMM Configuration (Two CPUs)

Figure 3-4 shows the configuration of DIMMs when two CPUs (CPU1 and CPU2) are configured for the NCS6742G N4 server.

**Figure 3-4 Recommended DIMM Configuration (Two CPUs)**

| DDR5 Qty | D | CPU1_D0 | CPU1_D1 | CPU1_C0 | CPU1_C1 | CPU1_B0 | CPU1_B1 | A | CPU1_A0 | CPU1_A1 | E       | F       | G       | H       | D       | C       | B       | A       | E       | F       | G       | H       |         |         |         |
|----------|---|---------|---------|---------|---------|---------|---------|---|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|
|          |   |         |         |         |         |         |         |   |         |         | CPU1_E1 | CPU1_E0 | CPU1_F1 | CPU1_F0 | CPU1_G1 | CPU1_G0 | CPU1_H1 | CPU1_H0 | CPU2_E1 | CPU2_E0 | CPU2_F1 | CPU2_F0 | CPU2_G1 | CPU2_G0 | CPU2_H1 |
| 2        | - | -       | -       | -       | -       | -       | -       | - | ✓       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       |         |
| 4        | - | -       | -       | -       | -       | -       | -       | - | ✓       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       |         |
| 6        | - | -       | ✓       | -       | -       | -       | -       | - | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       |         |
| 8        | - | -       | ✓       | -       | -       | -       | -       | - | ✓       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       |         |
| 10       | - | -       | ✓       | -       | -       | -       | -       | - | ✓       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       |         |
| 12       | ✓ | -       | ✓       | -       | -       | -       | -       | - | ✓       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       |         |
| 16       | ✓ | -       | ✓       | -       | ✓       | -       | ✓       | - | ✓       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       |         |
| 24       | ✓ | -       | ✓       | ✓       | ✓       | -       | ✓       | ✓ | ✓       | ✓       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       |         |
| 32       | ✓ | ✓       | ✓       | ✓       | ✓       | ✓       | ✓       | ✓ | ✓       | ✓       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       | -       |         |

- "-✓" indicates to install a DIMM.
- "-" indicates not to install a DIMM.



When two CPUs are configured, it is not recommended that you install an odd number of DIMMs.

## 3.6 Memory Protection Technologies

DDR5 DIMMs support the following memory protection technologies:

- Error Check and Correction ([ECC](#))
- On-die ECC
- Error Check and Scrub ([ECS](#))

- Memory Mirroring
- Memory Single Device Data Correction ([SDDC](#))
- Failed [DIMM](#) Isolation
- Memory Thermal Throttling
- Command/Address Parity Check and Retry
- Memory Demand/Patrol Scrubbing
- Memory Data Scrambling
- Post Package Repair ([PPR](#))
- Write Data [CRC](#) Protection
- Adaptive Data Correction - Single Region (ADC-SR)
- Adaptive Double Device Data Correction - Multiple Region ([ADDDC-MR](#))
- Partial Cache Line Sparing ([PCLS](#), [HBM](#) CPU only)

# Chapter 4

# Storage

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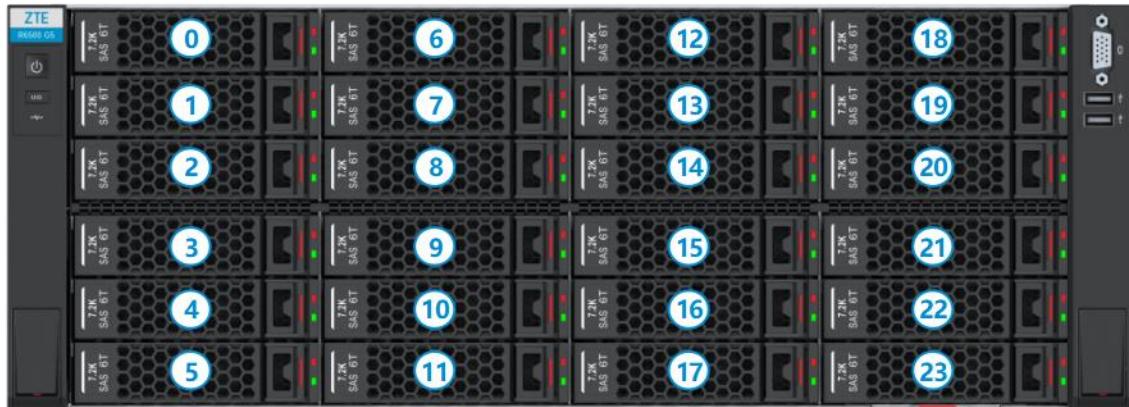
## 4.1 Hard Disk Slot

The NCS6742G N4 server supports installation of hard disks on its front panel. In accordance with the layout (horizontal and vertical) and number of hard disks, the NCS6742G N4 server provides the following hard disk configuration modes:

- Horizontal layout (24 hard disks)

Figure 4-1 shows the hard disk slots arranged when 24 hard disks are installed horizontally.

Figure 4-1 Horizontal Layout (24 Hard Disk Slots)

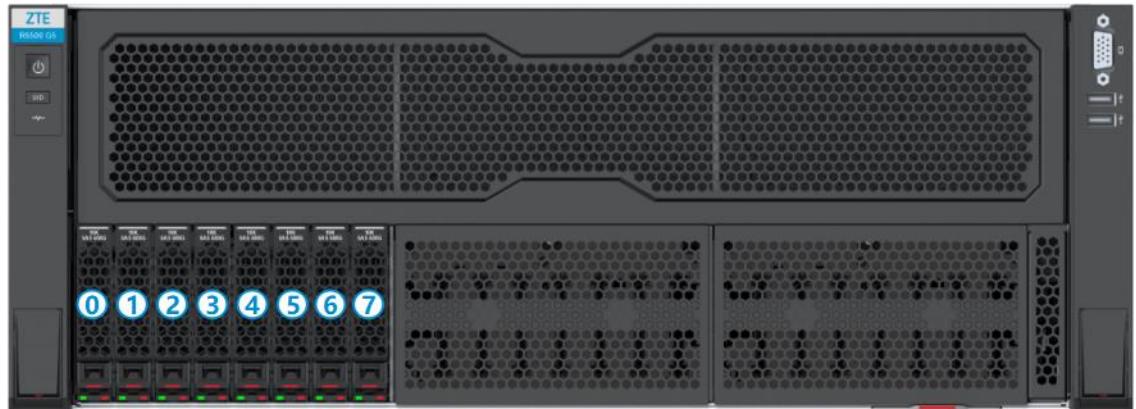


All slots support [SAS/SATA](#) hard disks. In addition, slots 0–7 also support [NVMe](#) hard disks.

- Vertical layout (8 hard disks)

Figure 4-2 shows the hard disk slots arranged when 8 hard disks are installed vertically.

Figure 4-2 Vertical Layout (8 Hard Disk Slots)

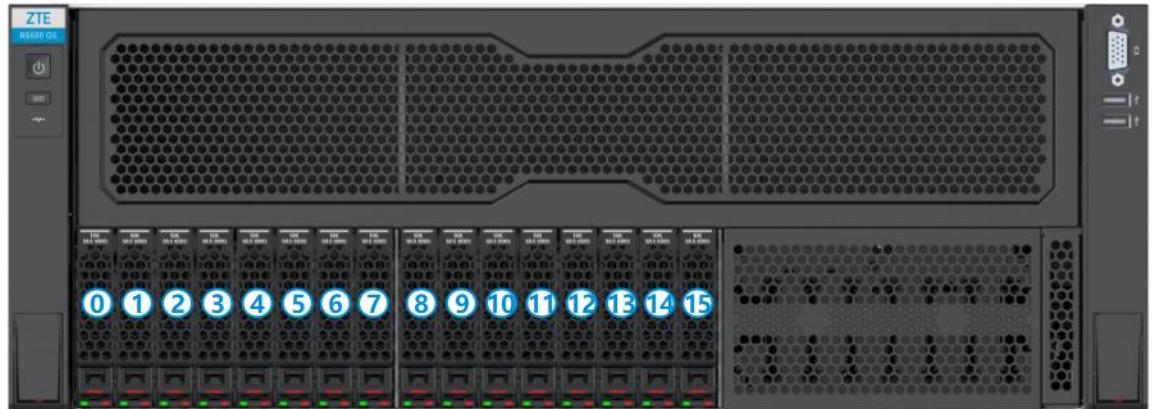


All slots support SAS/SATA/NVMe hard disks.

- Vertical layout (16 hard disks)

Figure 4-3 shows the hard disk slots arranged when 16 hard disks are installed vertically.

Figure 4-3 Vertical Layout (16 Hard Disk Slots)

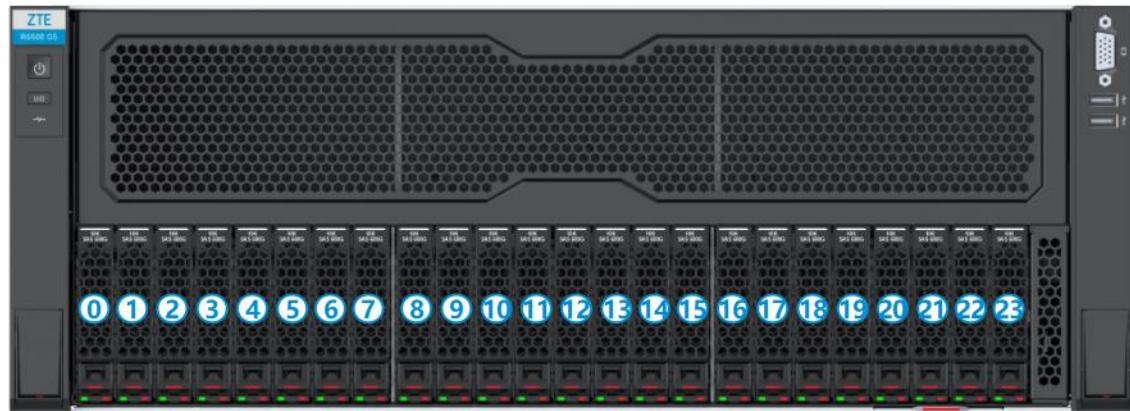


All slots support SAS/SATA hard disks. In addition, slots 0–11 also support NVMe hard disks.

- Vertical layout (24 hard disks)

Figure 4-4 shows the hard disk slots arranged when 24 hard disks are installed vertically.

**Figure 4-4 Vertical Layout (24 Hard Disk Slots)**

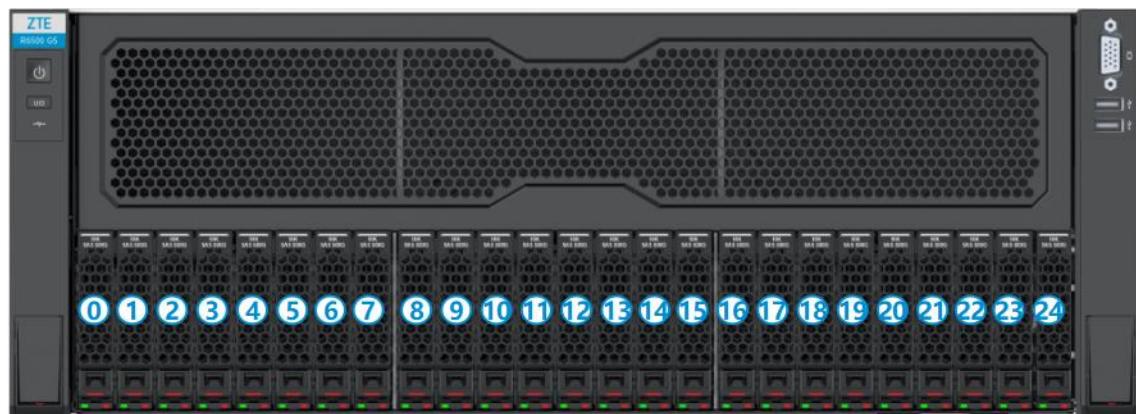


All slots support SAS/SATA hard disks. In addition, slots 0–11 also support NVMe hard disks.

- Vertical layout (25 hard disks)

Figure 4-5 shows the hard disk slots arranged when 25 hard disks are installed vertically.

**Figure 4-5 Vertical Layout (25 Hard Disk Slots)**



All slots support SAS/SATA hard disks. In addition, slots 1, 3, 5, 7, 17, 19, 21, and 23 also support NVMe hard disks.



To ensure drive availability, the storage duration of a hard disk drive cannot exceed six months before use.

## 4.2 Hard Disk Indicator

Figure 4-6 shows the hard disk indicators on the NCS6742G N4 server.

**Figure 4-6 Hard Disk Indicators**

1. Hard disk status indicator
2. Hard disk activity indicator

For a description of the hard disk indicators, refer to [Table 4-1](#).

**Table 4-1 Hard Disk Indicator Descriptions**

| Indicator                    | Status  |
|------------------------------|---|
| Hard disk status indicator   | The possible status of the indicator is one of the following: <ul style="list-style-type: none"> <li>● Off: The hard disk is operating properly.</li> <li>● Flashing blue at 1 Hz: The <a href="#">RAID</a> group that the hard disk belongs to is being rebuilt.</li> <li>● Flashing blue at 4 Hz: The hard disk is being positioned.</li> <li>● Steady red: The hard disk is faulty.</li> </ul>   |
| Hard disk activity indicator | The possible status of the indicator is one of the following: <ul style="list-style-type: none"> <li>● Off: The hard disk is not present or is faulty.</li> <li>● Flashing green: Data is being read from or written to the hard disk, or synchronized between hard disks. (The indicator flashes green at 4 Hz on a <a href="#">SAS/SATA</a> disk and flashes green at an undefined frequency on an <a href="#">NVMe</a> disk.)</li> <li>● Steady green: The hard disk is present but inactive.</li> </ul> |

## 4.3 RAID Controller Card

Through a [RAID](#) controller card of the corresponding model, the [RAID](#) technology combines multiple independent hard disks to form an array with the redundancy capability. Compared with a single hard disk, the [RAID](#) array provides higher storage performance, [I/O](#) performance, and reliability.

The [RAID](#) controller card provides the functions such as [RAID](#) support, [RAID](#) level migration, and disk roaming.

For detailed information about [RAID](#) controller cards, refer to the *NETAS Server [RAID](#) User Guide (Intel EagleStream)*.

# Chapter 5

# Network

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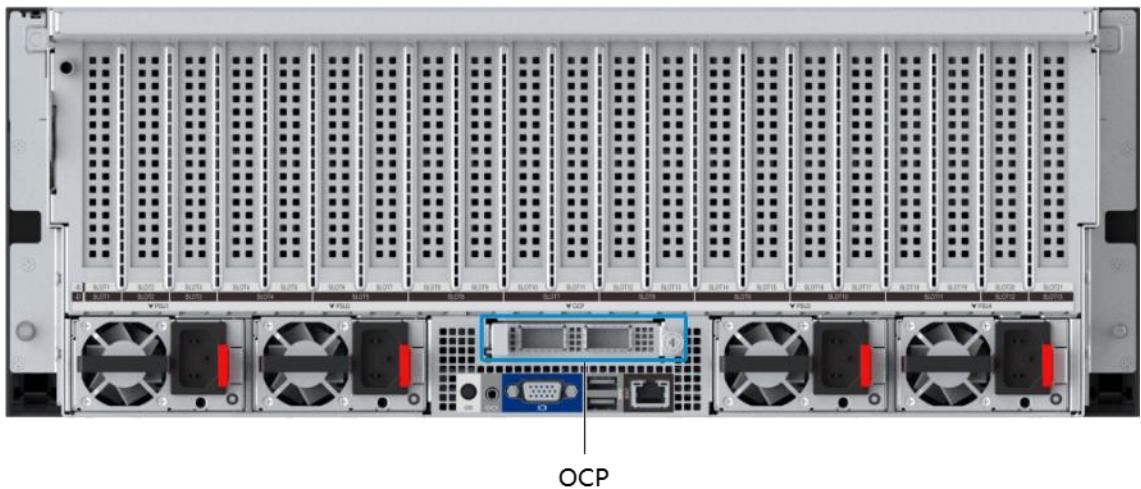
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### 5.1 OCP NIC

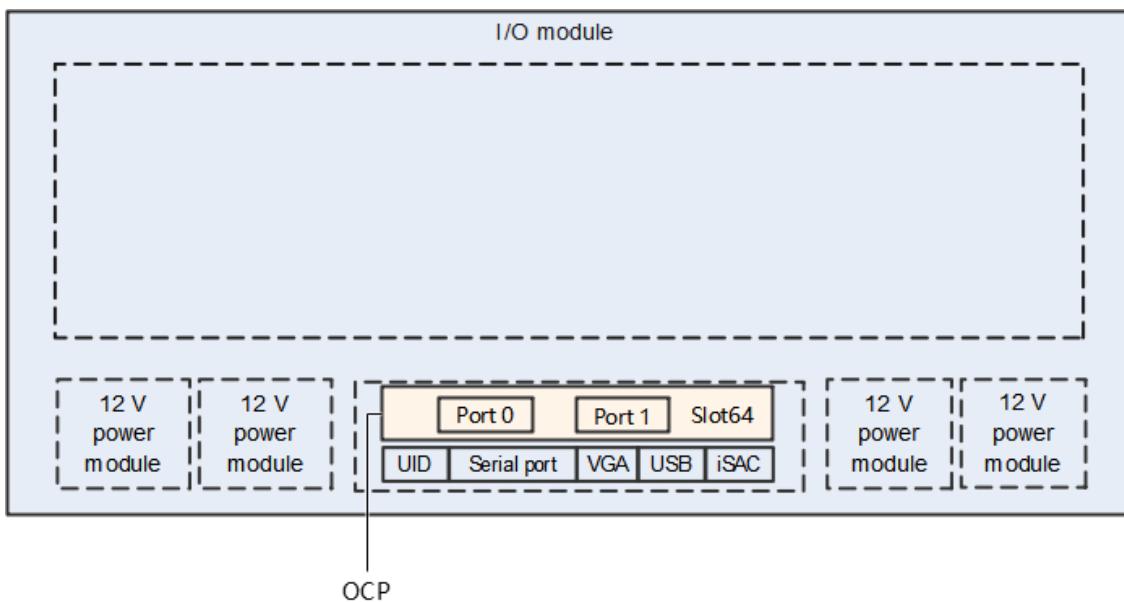
The NCS6742G N4 server supports [OCP NICs](#) to provide more network capabilities. [Figure 5-1](#) shows the position of the OCP NICs.

[Figure 5-1 OCP NIC Position](#)



The port names of an OCP NIC configured for the NCS6742G N4 server are usually determined by the [BIOS](#). Some [OSs](#) support customization of the port names. By default, a port name of an OCP NIC configured for the NCS6742G N4 server is `ensxy`. In the port name, `x` indicates the slot ID of the OCP NIC and `y` indicates the port ID. (The left port of the OCP NIC is numbered 0, which is incremented by one on the right.)

[Figure 5-2](#) shows the IDs of the ports provided by each OCP NIC when the NCS6742G N4 server is configured with OCP NICs that have two optical interfaces each.

**Figure 5-2 OCP NIC Configuration**

In [Figure 5-2](#), the ports of the OCP NIC located in slot 64 are named `ens64f0` and `ens64f1`.

For the OCP NIC models that the NCS6742G N4 server supports, refer to [Table 5-1](#).

**Table 5-1 Supported OCP NIC Models**

| OCP NIC Model        | Network Port Type    | Number of Network Ports | Rate     | NC-SI/WOL/PXE Supported Or Not |
|----------------------|----------------------|-------------------------|----------|--------------------------------|
| E810-XXVDA2 (983263) | Optical interface    | 2                       | 25 Gbps  | Supported                      |
| X710DA2              | Optical interface    | 2                       | 10 Gbps  | Supported                      |
| X710T2L              | Electrical interface | 2                       | 10 Gbps  | Supported                      |
| MCX562A-ACAB         | Optical interface    | 2                       | 25 Gbps  | Supported                      |
| MCX566A-CDAB         | Optical interface    | 2                       | 100 Gbps | Supported                      |
| MCX4621A-XCAB        | Optical interface    | 2                       | 10 Gbps  | Supported                      |
| MCX623436AN-CDAB     | Optical interface    | 2                       | 100 Gbps | Supported                      |

**Note**

The number of OCP NIC models supported by the NCS6742G N4 server is growing. For more information, contact technical support.

## 5.2 PCIe NIC

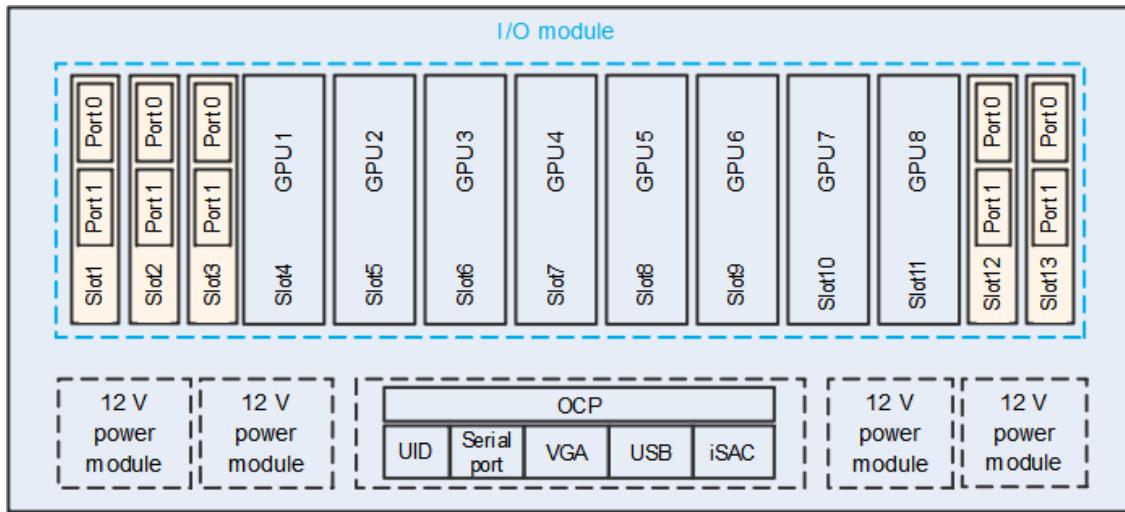
A [PCIe NIC](#) is a network adapter that provides PCIe ports. It is connected to the mainboard through a PCIe port.

The NCS6742G N4 server supports PCIe NICs to provide more network capabilities.

The port names of a PCIe NIC configured for the NCS6742G N4 server are usually determined by the [BIOS](#). Some [OSs](#) support customization of the port names. By default, a port name of a PCIe NIC configured for the NCS6742G N4 server is `ensxy`. In the port name, **x** indicates the slot ID of the PCIe NIC and **y** indicates the port ID. (The port far away from the gold finger of the PCIe NIC is numbered 0, which is incremented by one as the distance shortens.)

[Figure 5-3](#) shows the IDs of the ports provided by each PCIe NIC when the NCS6742G N4 server is configured with PCIe NICs that have two optical interfaces each.

**Figure 5-3 Typical PCIe NIC Configuration**



In [Figure 5-3](#), the ports of the PCIe NIC located in slot 1 are named `ens1f0` and `ens1f1`.

PCIe NICs support smart NICs and common NICs.

- For the smart NIC models that the NCS6742G N4 server supports, refer to [Table 5-2](#).

**Table 5-2 Supported Smart NIC Models**

| Smart NIC Model | Network Port Type | Number of Network Ports | Rate     | Supported PCIe Rate |
|-----------------|-------------------|-------------------------|----------|---------------------|
| MBF2H512C-AEUOT | Optical interface | 2                       | 25 Gbps  | PCIe 4.0 x16        |
| MBF2H516A-CENOT | Optical interface | 2                       | 100 Gbps | PCIe 4.0 x16        |
| MBF2H516C-CESOT | Optical interface | 2                       | 100 Gbps | PCIe 4.0 x16        |

**Note**

The number of smart NIC models supported by the NCS6742G N4 server is growing. For more information, contact technical support.

- For the common NIC models that the NCS6742G N4 server supports, refer to [Table 5-3](#).

**Table 5-3 Supported Common NIC Models**

| Common NIC Model           | Network Port Type    | Number of Network Ports | Rate    | Supported PCIe Rate |
|----------------------------|----------------------|-------------------------|---------|---------------------|
| NS214                      | Optical interface    | 2                       | 10 Gbps | PCIe 3.0 x8         |
| NS312                      | Optical interface    | 2                       | 25 Gbps | PCIe 3.0 x8         |
| NS212                      | Optical interface    | 2                       | 25 Gbps | PCIe 3.0 x8         |
| Intel I350T2G2P20 (934607) | Electrical interface | 2                       | 1 Gbps  | PCIe 2.0 x4         |
| Intel I350T4G2P20 (934608) | Electrical interface | 4                       | 1 Gbps  | PCIe 2.0 x4         |

**Note**

The number of common NIC models supported by the NCS6742G N4 server is growing. For more information, contact technical support.

# Chapter 6

# I/O Expansion

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## 6.1 PCIe Card

PCIe cards are connected to the mainboard through the PCIe switch board to provide system expansion capabilities. PCIe cards can be configured as required.



### Note

- For a description of the PCIe switch board, refer to [9.3 Switch Boards](#).
- For a description of the mainboard, refer to [9.2 Mainboard](#).

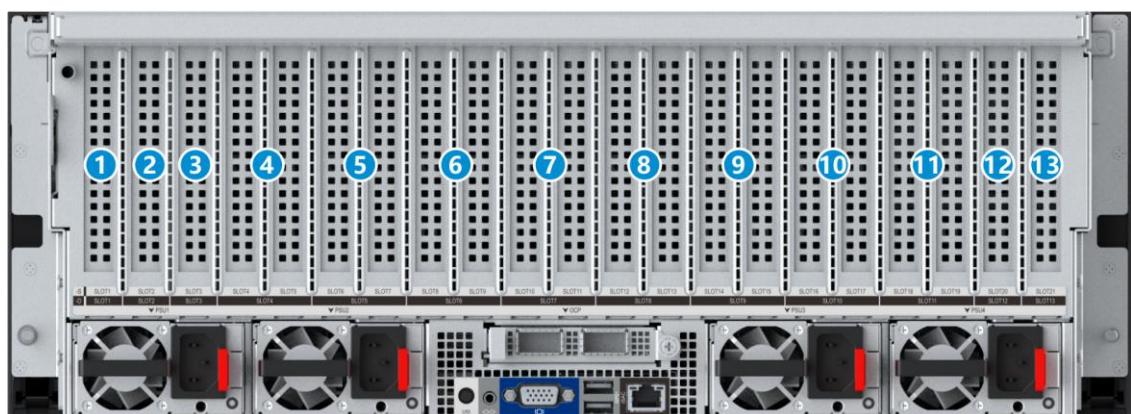
## 6.2 PCIe Card Slots and Descriptions

The I/O module of the NCS6742G N4 server supports the following configurations:

- 13 PCIe 4.0/5.0 slots

[Figure 6-1](#) shows the PCIe card slots of the NCS6742G N4server with this configuration.

**Figure 6-1 13 PCIe 4.0/5.0 Slots**





The numbers in [Figure 6-1](#) indicate PCIe slot IDs.

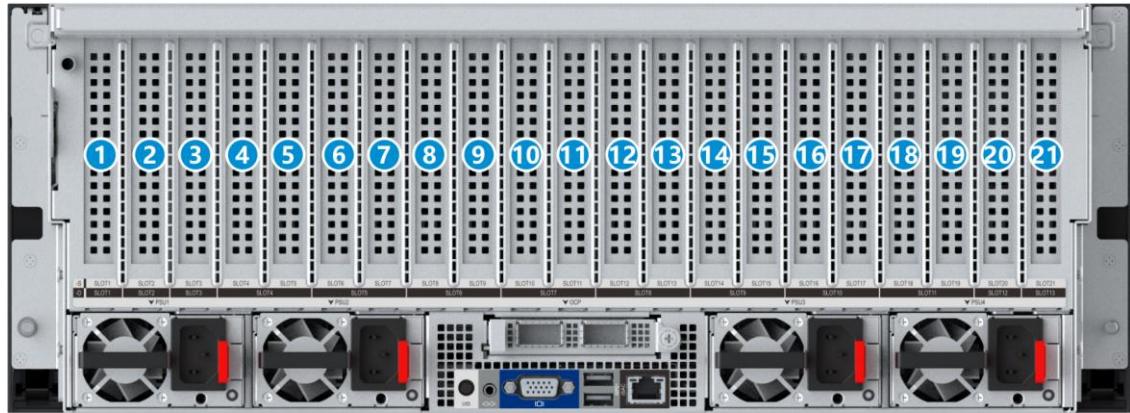
For a description of the PCIe card types that can be configured in each slot, refer to [Table 6-1](#).

**Table 6-1 PCIe Card Slot Descriptions—13 PCIe 4.0/5.0 Slots**

| Configuration Mode   | Slot ID             | PCIe Card Type                 |
|--|---------------------|--------------------------------|
| 10 dual-slot GPUs + 1 single-slot standard PCIe card                           | Slot1               | Single-slot standard PCIe card |
|  | Slot 2 and Slot 3   | Dual-slot GPU                  |
|  | Slot 4–Slot 11      | Dual-slot GPU                  |
|  | Slot 12 and Slot 13 | Dual-slot GPU                  |
| 8 dual-slot GPUs + 5 single-slot standard PCIe cards                           | Slot1–Slot3         | Single-slot standard PCIe card |
|  | Slot 4–Slot 11      | Dual-slot GPU                  |
|  | Slot 12 and Slot 13 | Single-slot standard PCIe card |
| 8 dual-slot GPUs + 1 single-slot smart NIC + 4 single-slot standard PCIe cards | Slot1               | Single-slot smart NIC          |
|  | Slot 2 and Slot 3   | Single-slot standard PCIe card |
|  | Slot 4–Slot 11      | Dual-slot GPU                  |
|  | Slot 12 and Slot 13 | Single-slot standard PCIe card |
| 8 dual-slot GPUs + 1 dual-slot smart NIC + 3 single-slot standard PCIe cards   | Slot 1 and Slot 2   | Dual-slot smart NIC            |
|  | Slot3               | Single-slot standard PCIe card |
|  | Slot 4–Slot 11      | Dual-slot GPU                  |
|  | Slot 12 and Slot 13 | Single-slot standard PCIe card |

- 21 PCIe 4.0 slots

[Figure 6-2](#) shows the PCIe card slots of the server with this configuration.

**Figure 6-2 21 PCIe 4.0 Slots****Note**

The numbers in [Figure 6-2](#) indicate PCIe slot IDs.

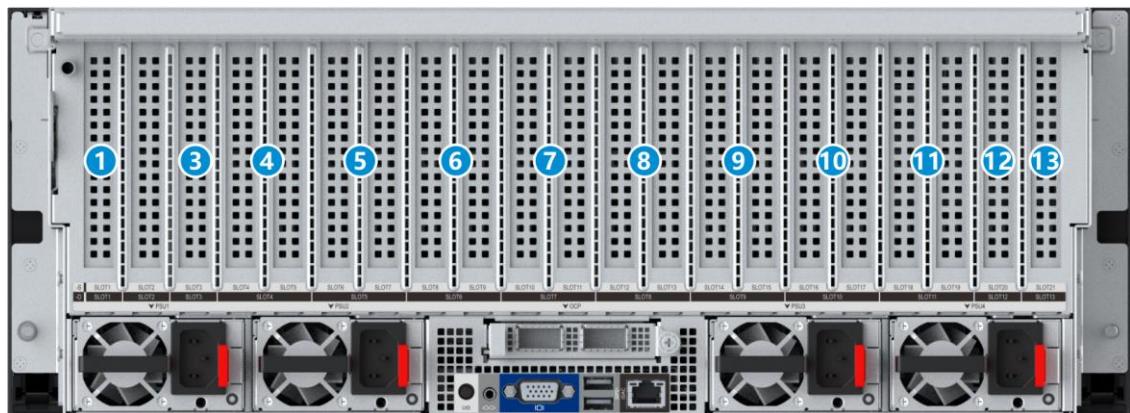
For a description of the PCIe card types that can be configured in each slot, refer to [Table 6-2](#).

**Table 6-2 PCIe Card Slot Descriptions—21 PCIe 4.0 Slots**

| Configuration Mode                                    | Slot ID             | PCIe Card Type                 |
|---|---------------------|--------------------------------|
| 16 dual-slot GPUs + 5 single-slot standard PCIe cards | Slot 1–Slot 3       | Single-slot standard PCIe card |
|   | Slot 4–Slot 19      | Single-slot GPU                |
|   | Slot 20 and Slot 21 | Single-slot standard PCIe card |

- 12 PCIe 5.0 slots

[Figure 6-3](#) shows the PCIe card slots of the server with this configuration.

**Figure 6-3 12 PCIe 5.0 Slots**

**Note**

Compared with the configuration with 13 PCIe 4.0/5.0 slots, the only difference is that Slot 2 is unavailable in the configuration with 12 PCIe 5.0 slots.

For a description of the PCIe card types that can be configured in each slot, refer to [Table 6-3](#).

**Table 6-3 PCIe Card Slot Descriptions—12 PCIe 5.0 Slots**

| Configuration Mode   | Slot ID             | PCIe Card Type                 |
|--|---------------------|--------------------------------|
| 8 single-slot/dual-slot GPUs + 4 single-slot standard PCIe cards | Slot 1 and Slot 3   | Single-slot standard PCIe card |
|  | Slot 4–Slot 11      | Single-slot/dual-slot GPU      |
|  | Slot 12 and Slot 13 | Single-slot standard PCIe card |

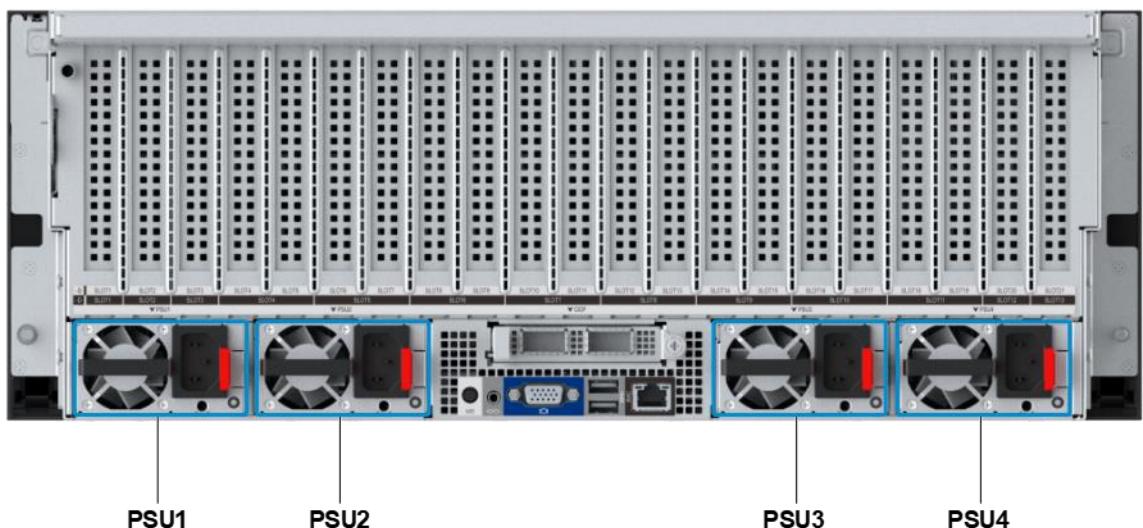
# Chapter 7

## Power Module

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[Figure 7-1](#) shows the positions of the power modules on the NCS6742G N4 server.

**Figure 7-1 Power Module Positions**



The power module configurations of the NCS6742G N4 server are described as follows:

- Various types of power modules (for example, 800 W, 1300 W, 2000 W, 2700 W, and 3200 W), including platinum power modules, are supported.
- The 100 V–127 V and 200 V–240 V (50 Hz to 60 Hz) [AC](#) power input is supported.
- The 240 V and 336 V high-voltage [DC](#) power input is supported.
- The –48 V low-voltage DC power input is supported.
- Two or four power modules are supported.
- Hot swapping is supported.
- The 2+2 redundancy mode is supported when four power modules are configured.
- The power modules installed on the same server must be of the same model.
- The power modules are protected against short circuits.

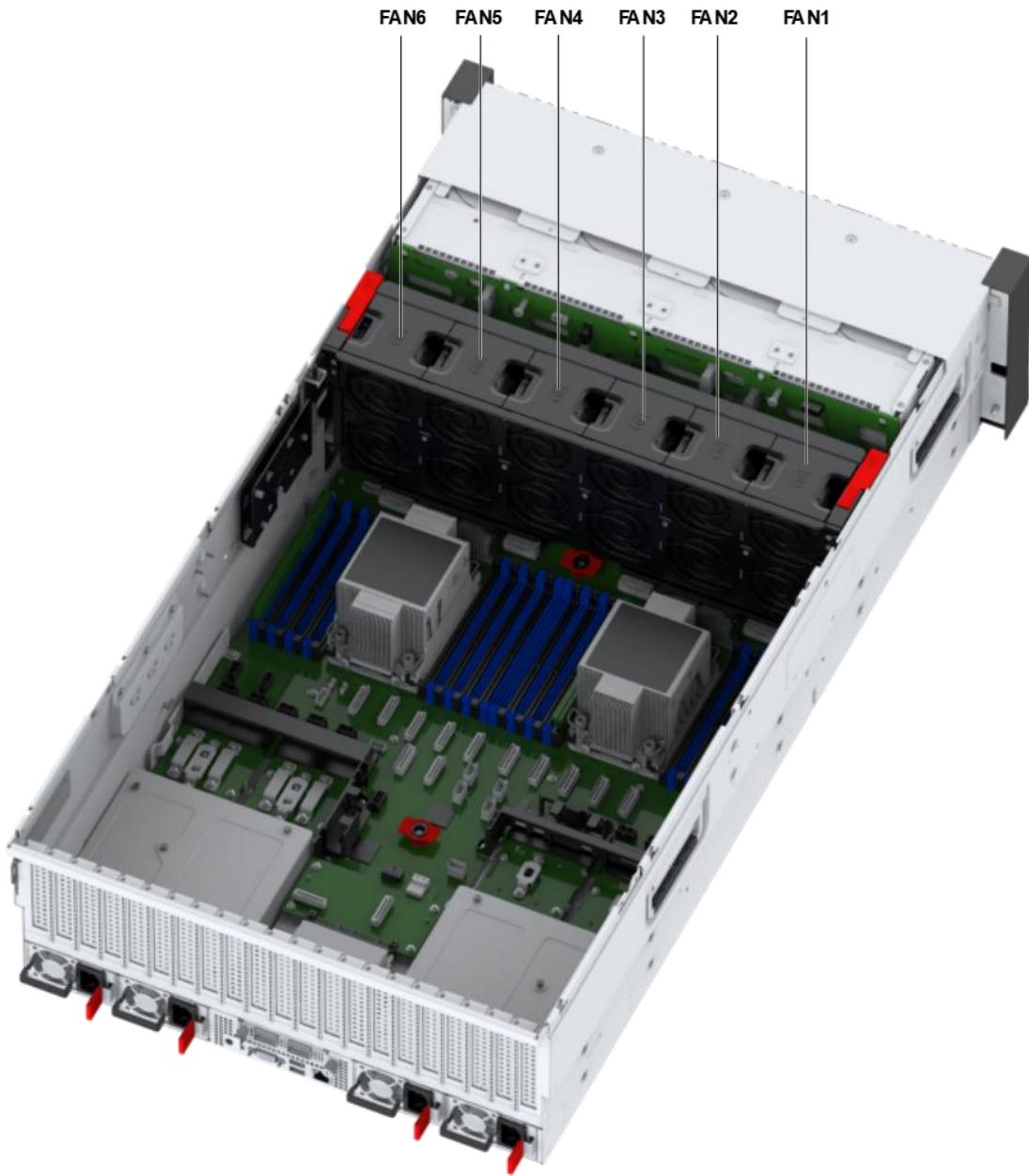
# Chapter 8

## Fan Unit

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[Figure 8-1](#) shows the positions of fan units on the NCS6742G N4 server.

**Figure 8-1 Fan Unit Positions**



The fan unit configurations of the NCS6742G N4 server are described as follows:

- Six fan units (FAN1–FAN6) are supported, and each fan unit consists of two fans.
  - ➔ FAN1: The two fans are numbered 1 and 2 from top to bottom.
  - ➔ FAN2: The two fans are numbered 3 and 4 from top to bottom.
  - ➔ FAN3: The two fans are numbered 5 and 6 from top to bottom.
  - ➔ FAN4: The two fans are numbered 7 and 8 from top to bottom.
  - ➔ FAN5: The two fans are numbered 9 and 10 from top to bottom.
  - ➔ FAN6: The two fans are numbered 11 and 12 from top to bottom.

- The server supports two fan specifications: 8038 and 8056.

---

**Note**

The fans installed on a server must be of the same model and specification.

- Hot swapping is supported.
- If a fan fails, the corresponding fan unit can still operate properly.
- The fan speed is adjustable.

# Chapter 9

# Boards

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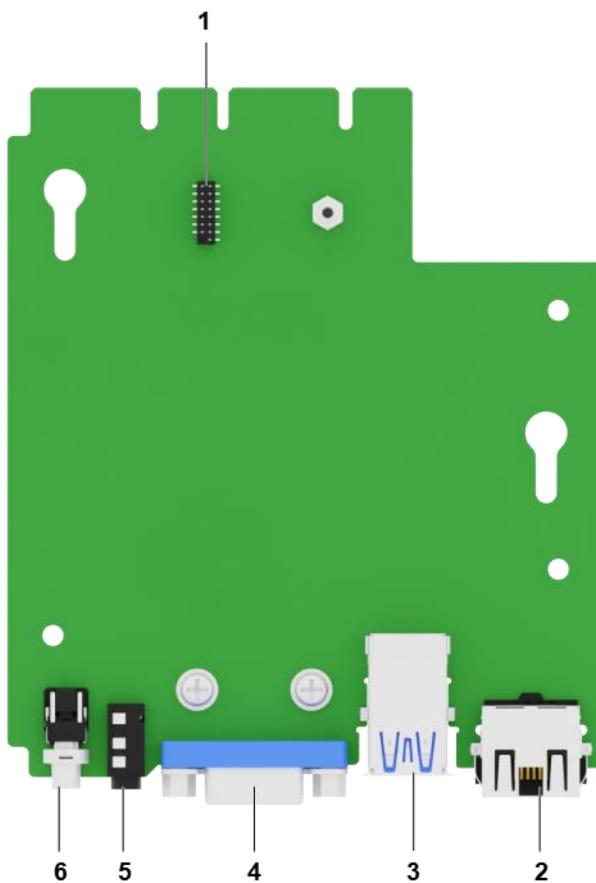
|                      |    |
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## 9.1 I/O Card

CPUs communicate with other devices through interfaces. Different devices have different interfaces, which are called **I/O** interfaces.

An I/O card is connected to the mainboard, and provides a network interface, **VGA** interface, and **USB** interfaces for external devices.

Figure 9-1 shows the I/O card of the NCS6742G N4 server.

**Figure 9-1 I/O Card**

For a description of the interfaces on the I/O card of the NCS6742G N4 server, refer to [Table 9-1](#).

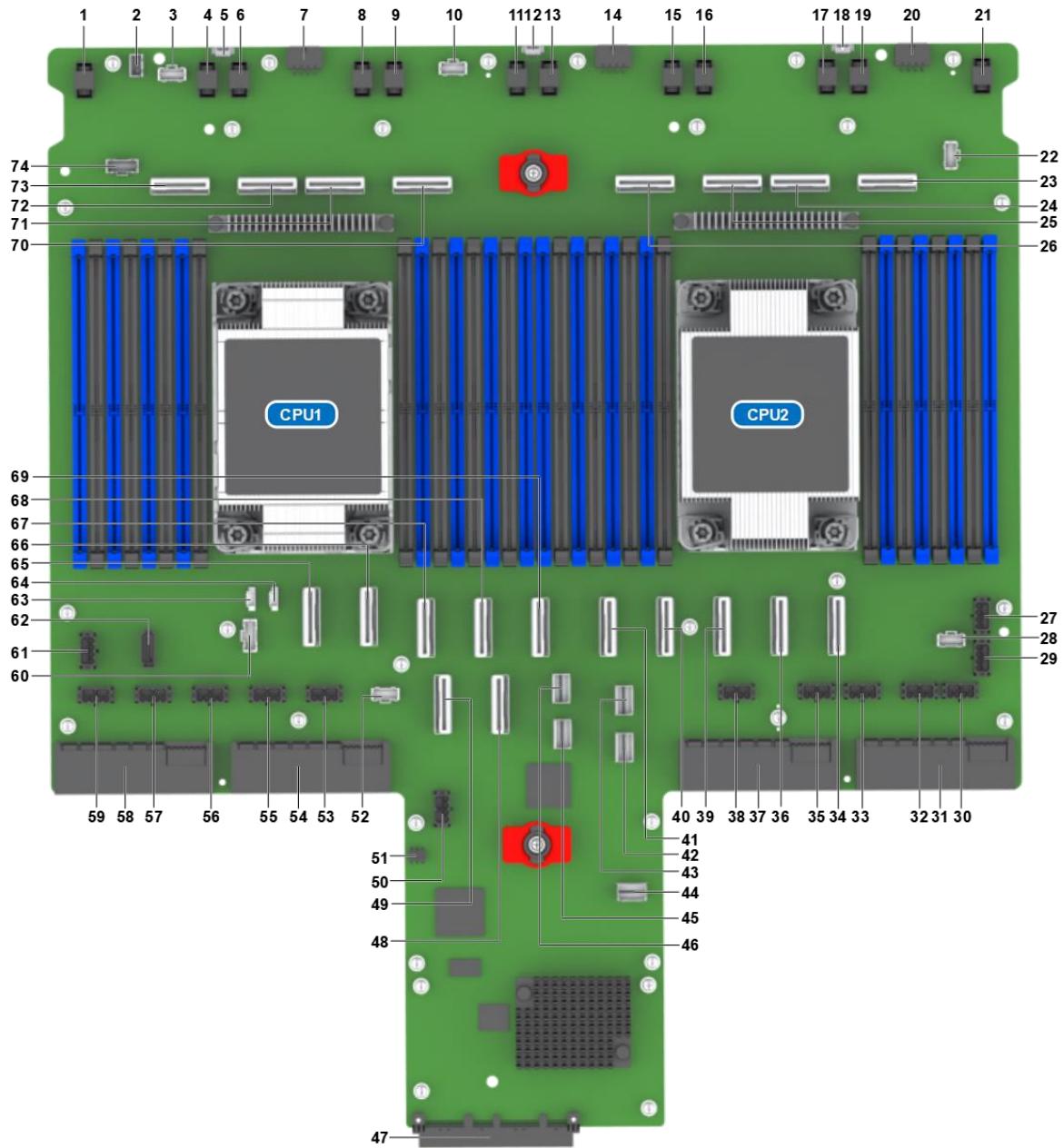
**Table 9-1 I/O Card Interface Descriptions**

| No. | Interface Name              | Silk Screen | Position Number |
|-----|-----------------------------|-------------|-----------------|
| 1   | TPM card interface          | TPM CARD    | X2              |
| 2   | BMC management network port | BMC_ETH     | X4              |
| 3   | USB 3.0 interface x 2       | USB1/USB2   | X6              |
| 4   | VGA interface               | VGA         | X7              |
| 5   | 3.5mm audio jack            | COM         | X3              |
| 6   | UID button and indicator    | UID         | S1              |

## 9.2 Mainboard

[Figure 9-2](#) shows the mainboard of the NCS6742G N4 server.

**Figure 9-2 Mainboard**



For a description of the interfaces on the mainboard of the NCS6742G N4, refer to [Table 9-2](#).

**Table 9-2 Mainboard Interface Descriptions**

| No. | Interface Name                       | Silk Screen  | Position Number |
|-----|--------------------------------------|--------------|-----------------|
| 1   | Fan unit interface 12                | FAN12        | X79             |
| 2   | Intrusion detection switch interface | INTRUDER     | X43             |
| 3   | Disk backplane retimer interface     | RETIMER_CARD | X40             |
| 4   | Fan unit interface 11                | FAN11        | X59             |

| No. | Interface Name  | Silk Screen    | Position Number |
|-----|---|----------------|-----------------|
| 5   | Disk backplane I2C interface 3                                      | I2C_BP3        | X12             |
| 6   | Fan unit interface 10   | FAN10          | X81             |
| 7   | Disk backplane power interface 3                                    | P12V_BP3       | X21             |
| 8   | Fan unit interface 9  | FAN9           | X80             |
| 9   | Fan unit interface 8  | FAN8           | X66             |
| 10  | Disk backplane expansion interface                                  | EXPANDER       | X84             |
| 11  | Fan unit interface 7  | FAN7           | X68             |
| 12  | Disk backplane I2C interface 2                                      | I2C_BP2        | X25             |
| 13  | Fan unit interface 6  | FAN6           | X67             |
| 14  | Disk backplane power interface 2                                    | P12V_BP2       | X19             |
| 15  | Fan unit interface 5  | FAN5           | X69             |
| 16  | Fan unit interface 4  | FAN4           | X63             |
| 17  | Fan unit interface 3  | FAN3           | X65             |
| 18  | Disk backplane I2C interface 1                                      | I2C_BP1        | X22             |
| 19  | Fan unit interface 2  | FAN2           | X64             |
| 20  | Disk backplane power interface 1                                    | P12V_BP1       | X17             |
| 21  | Fan unit interface 1  | FAN1           | X62             |
| 22  | Left lug interface  | FP_BIN/LED     | X45             |
| 23  | NVMe SSD PCIe x8 interface  | CPU2_HSIO8     | X13             |
| 24  | NVMe SSD PCIe x8 interface  | CPU2_HSIO7     | X18             |
| 25  | NVMe SSD PCIe x8 interface  | CPU2_HSIO6     | X50             |
| 26  | NVMe SSD PCIe x8 interface  | CPU2_HSIO5     | X49             |
| 27  | RAID controller card power interface                                | P12V_RAID      | X74             |
| 28  | RAID controller card communication interface                        | LINK_RAID      | X15             |
| 29  | Switch board power interface  | P12V_SW2       | X78             |
| 30  | Power interface 10 (co-shared by the GPU and the PCIe switch board) | P12V_GPU10_SW4 | X72             |
| 31  | PSU interface 4   | PSU4           | X4A2            |
| 32  | GPU power interface 8   | P12V_GPU8      | X71             |

| No. | Interface Name   | Silk Screen  | Position Number |
|-----|--|--------------|-----------------|
| 33  | GPU power interface 7                                  | P12V_GPU7    | X26             |
| 34  | PCIe x8 interface for the GPU on the PCIe switch board | CPU2_HSIO16  | X54             |
| 35  | GPU power interface 6                                  | P12V_GPU6    | X6              |
| 36  | PCIe x8 interface for the GPU on the PCIe switch board | CPU2_HSIO15  | X53             |
| 37  | PSU interface 3  | PSU3         | X3A2            |
| 38  | GPU power interface 5                                  | P12V_GPU5    | X10             |
| 39  | PCIe x8 interface for the GPU on the PCIe switch board | CPU2_HSIO14  | X70             |
| 40  | PCIe x8 interface for the GPU on the PCIe switch board | CPU2_HSIO13  | X55             |
| 41  | RAID controller card PCIe x8 interface                 | CPU2_HSIO18  | X28             |
| 42  | SATA interface 1                                       | PCH_SATA1    | X52             |
| 43  | SATA interface 2                                       | PCH_SATA2    | X3              |
| 44  | OCP card NCSI  | NCSI_OCP     | X16             |
| 45  | SATA interface 3                                       | PCH_SATA3    | X23             |
| 46  | M.2 interface  | PCH_SATA4_M2 | X83             |
| 47  | I/O card interface                                     | IO_CARD      | X24             |
| 48  | RAID controller card PCIe x8 interface                 | CPU2_HSIO20  | X58             |
| 49  | OCP card PCIe x8 interface                             | CPU1_HSIO19  | X56             |
| 50  | OCP card power interface                               | P12V_OCP     | X57             |
| 51  | Commissioning interface                                | -            | X1A4            |
| 52  | Switch board communication interface                   | LINK_SW      | X76             |
| 53  | GPU power interface 4                                  | P12V_GPU4    | X5              |
| 54  | PSU interface 2  | PSU2         | X2A2            |
| 55  | GPU power interface 3                                  | P12V_GPU3    | X2              |
| 56  | GPU power interface 2                                  | P12V_GPU2    | X4              |
| 57  | GPU power interface 1                                  | P12V_GPU1    | X1              |
| 58  | PSU interface 1  | PSU1         | X1A2            |

| No. | Interface Name   | Silk Screen   | Position Number |
|-----|--|---------------|-----------------|
| 59  | Power interface 9 (co-shared by the GPU and the PCIe switch board) | P12V_GPU9_SW3 | X60             |
| 60  | Smart NIC NCSI   | NCSI_SMARTNIC | X35             |
| 61  | Switch board power interface                                       | P12V_SW1      | X77             |
| 62  | USB 3.0/USB 2.0 interface  | FP_USB4       | X11             |
| 63  | Commissioning interface  | -             | X61             |
| 64  | Commissioning interface  | -             | X31             |
| 65  | PCIe x8 interface for the GPU on the PCIe switch board             | CPU1_HSIO9    | X46             |
| 66  | PCIe x8 interface for the GPU on the PCIe switch board             | CPU1_HSIO10   | X42             |
| 67  | OCP card PCIe x8 interface   | CPU1_HSIO17   | X36             |
| 68  | PCIe x8 interface for the GPU on the PCIe switch board             | CPU1_HSIO11   | X41             |
| 69  | PCIe x8 interface for the GPU on the PCIe switch board             | CPU1_HSIO12   | X44             |
| 70  | NVMe SSD PCIe x8 interface   | CPU1_HSIO4    | X8              |
| 71  | NVMe SSD PCIe x8 interface   | CPU1_HSIO3    | X47             |
| 72  | PCIe x8 interface for the smart NIC on the PCIe switch board       | CPU1_HSIO2    | X48             |
| 73  | PCIe x8 interface for the smart NIC on the PCIe switch board       | CPU1_HSIO1    | X14             |
| 74  | Right lug interface  | FP_USB/VGA    | X20             |

## 9.3 Switch Boards

With a **PCIe** switch board, the server can provide a certain number of **PCIe** card slots for expanding system functions.

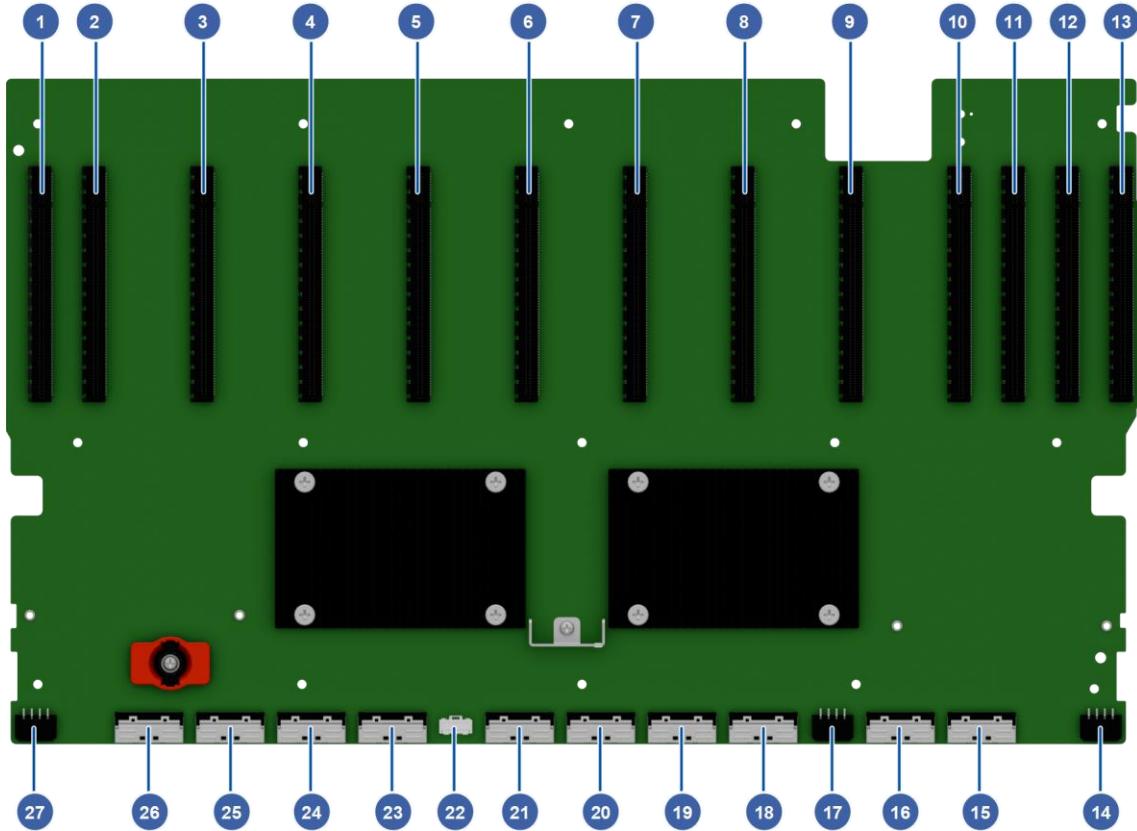
The NCS6742G N4 server supports the following PCIe switch boards:

- 13-slot PCIe 4.0 switch board SWP65N40A. For details, refer to [9.3.1 SWP65N40A](#).
- 13-slot PCIe 5.0 switch board SW6505P5A. For details, refer to [9.3.2 SW6505P5A](#).
- 21-slot PCIe 4.0 switch board SWP65N41A. For details, refer to [9.3.3 SWP65N41A](#).
- 12-slot PCIe 4.0 pass-through board SW6505PT4A. For details, refer to [9.3.4 SW6505PT4A](#).

### 9.3.1 SWP65N40A

Figure 9-3 shows the 13-slot PCIe 4.0 switch board SWP65N40A.

**Figure 9-3 SWP65N40A**



For a description of the interfaces on the 13-slot PCIe 4.0 switch board SWP65N40A, refer to [Table 9-3](#).

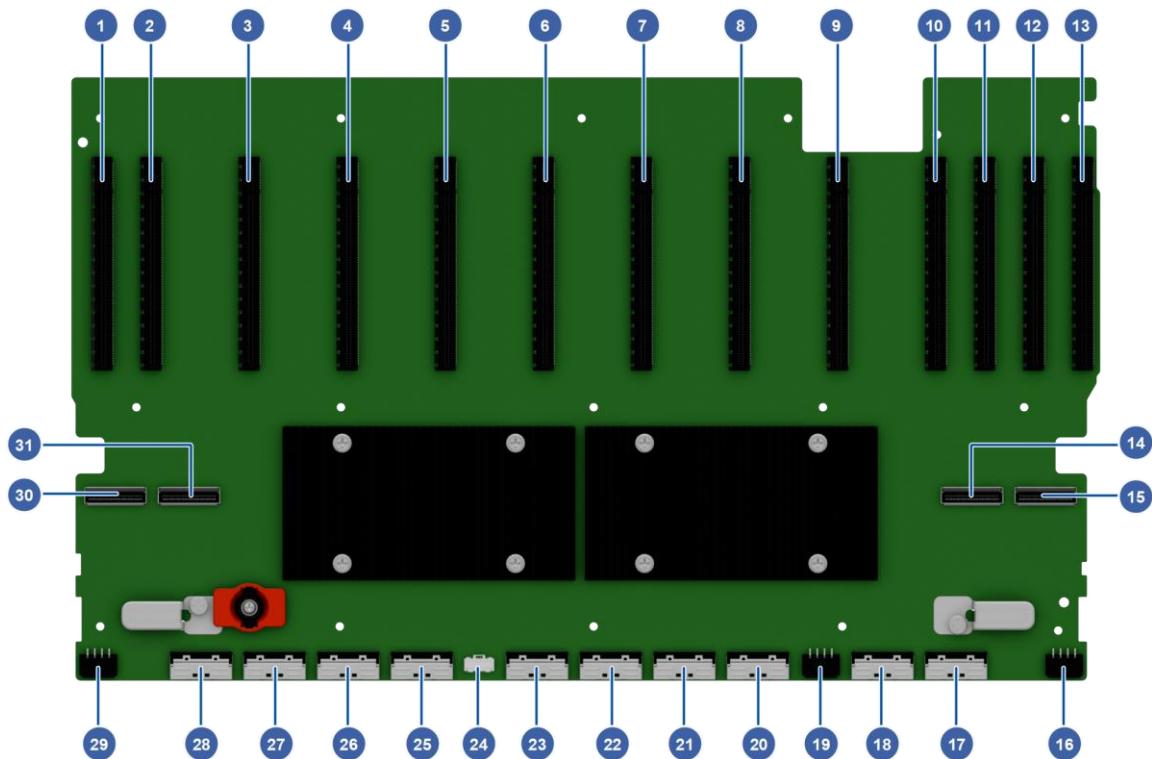
**Table 9-3 SWP65N40A Interface Descriptions**

| No. | Interface Name    | Silk Screen | Position Number |
|-----|-------------------|-------------|-----------------|
| 1   | PCIe interface 13 | SLOT 13     | X26             |
| 2   | PCIe interface 12 | SLOT 12     | X25             |
| 3   | PCIe interface 11 | SLOT 11     | X21             |
| 4   | PCIe interface 10 | SLOT 10     | X20             |
| 5   | PCIe interface 9  | SLOT 9      | X19             |
| 6   | PCIe interface 8  | SLOT 8      | X18             |
| 7   | PCIe interface 7  | SLOT 7      | X17             |
| 8   | PCIe interface 6  | SLOT 6      | X16             |
| 9   | PCIe interface 5  | SLOT 5      | X15             |

| No. | Interface Name                  | Silk Screen      | Position Number |
|-----|---------------------------------|------------------|-----------------|
| 10  | PCIe interface 4                | SLOT 4           | X14             |
| 11  | PCIe interface 3                | SLOT 3           | X23             |
| 12  | PCIe interface 2                | SLOT 2           | X22             |
| 13  | Smart NIC PCIe interface 1      | SLOT 1/PCIe GEN5 | X24             |
| 14  | Power interface 1               | P12V_SW1         | X12             |
| 15  | PCIe x8 interface 0             | SW_HSIO_0        | X5              |
| 16  | PCIe x8 interface 1             | SW_HSIO_1        | X7              |
| 17  | Smart NIC power cable interface | P12V_SMARTNIC    | X29             |
| 18  | PCIe x8 interface 2             | SW_HSIO_2        | X4              |
| 19  | PCIe x8 interface 3             | SW_HSIO_3        | X2              |
| 20  | PCIe x8 interface 4             | SW_HSIO_4        | X1              |
| 21  | PCIe x8 interface 5             | SW_HSIO_5        | X3              |
| 22  | Data communication interface    | LINK_SW          | X11             |
| 23  | PCIe x8 interface 6             | SW_HSIO_6        | X8              |
| 24  | PCIe x8 interface 7             | SW_HSIO_7        | X6              |
| 25  | PCIe x8 interface 8             | SW_HSIO_8        | X9              |
| 26  | PCIe x8 interface 9             | SW_HSIO_9        | X10             |
| 27  | Power interface 2               | P12V_SW2         | X13             |

### 9.3.2 SW6505P5A

Figure 9-4 shows the 13-slot PCIe 5.0 switch board SW6505P5A.

**Figure 9-4 SW6505P5A**

For a description of the interfaces on the 13-slot PCIe 5.0 switch board SW6505P5A, refer to [Table 9-4](#).

**Table 9-4 SW6505P5A Interface Descriptions**

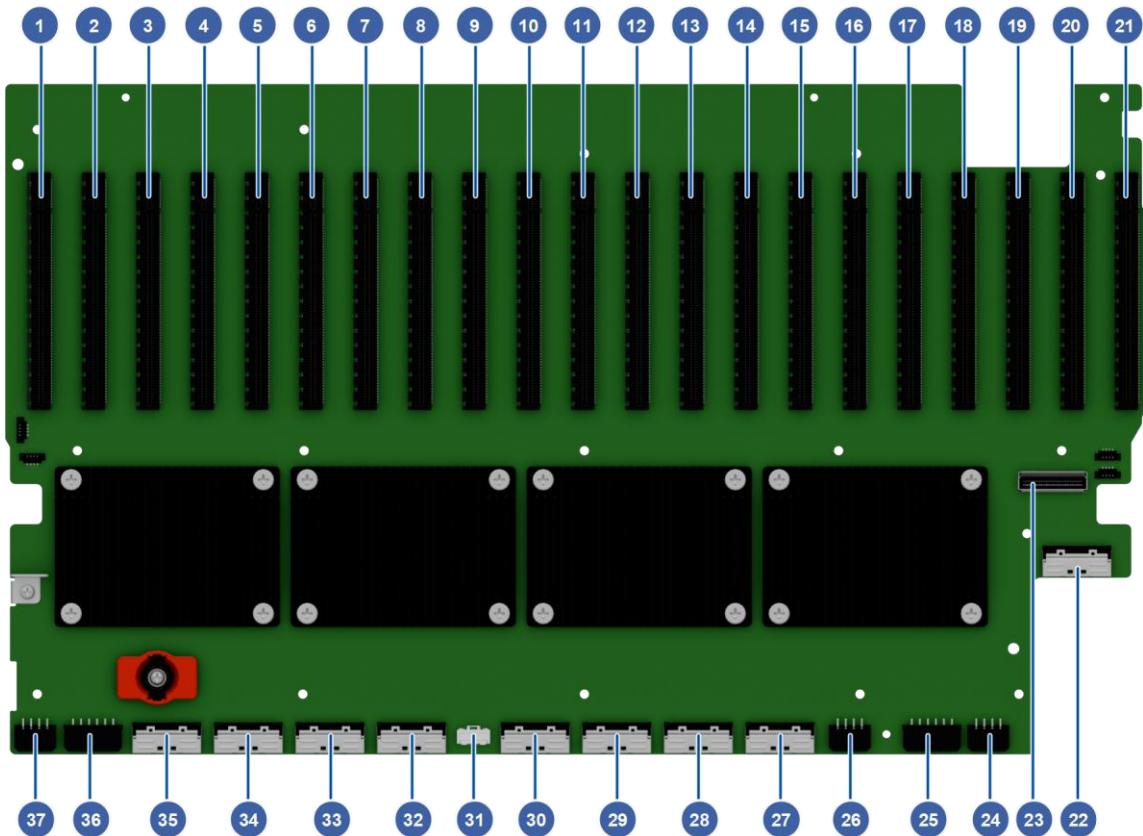
| No. | Interface Name    | Silk Screen           | Position Number |
|-----|-------------------|-----------------------|-----------------|
| 1   | PCIe interface 13 | SLOT 13/PCIE GEN5/X16 | X26             |
| 2   | PCIe interface 12 | SLOT 12/PCIE GEN5/X16 | X25             |
| 3   | PCIe interface 11 | SLOT 11/PCIE GEN5/X16 | X21             |
| 4   | PCIe interface 10 | SLOT 10/PCIE GEN5/X16 | X20             |
| 5   | PCIe interface 9  | SLOT 9/PCIE GEN5/X16  | X19             |
| 6   | PCIe interface 8  | SLOT 8/PCIE GEN5/X16  | X18             |
| 7   | PCIe interface 7  | SLOT 7/PCIE GEN5/X16  | X17             |
| 8   | PCIe interface 6  | SLOT 6/PCIE GEN5/X16  | X16             |
| 9   | PCIe interface 5  | SLOT 5/PCIE GEN5/X16  | X15             |
| 10  | PCIe interface 4  | SLOT 4/PCIE GEN5/X16  | X14             |
| 11  | PCIe interface 3  | SLOT 3/PCIE GEN5/X16  | X23             |
| 12  | PCIe interface 2  | SLOT 2/PCIE GEN5/X16  | X22             |

| No. | Interface Name                  | Silk Screen          | Position Number |
|-----|---------------------------------|----------------------|-----------------|
| 13  | Smart NIC PCIe interface 1      | SLOT 1/PCIE GEN5/X16 | X24             |
| 14  | PCIe x8 interface 0             | SW_HSIO_0            | X5              |
| 15  | PCIe x8 interface 1             | SW_HSIO_1            | X7              |
| 16  | Power interface 1               | P12V_SW1             | X12             |
| 17  | PCIe x8 interface 2             | SW_HSIO_2            | X4              |
| 18  | PCIe x8 interface 3             | SW_HSIO_3            | X2              |
| 19  | Smart NIC power cable interface | P12V_SMARTNIC        | X29             |
| 20  | PCIe x8 interface 4             | SW_HSIO_4            | X1              |
| 21  | PCIe x8 interface 5             | SW_HSIO_5            | X3              |
| 22  | PCIe x8 interface 6             | SW_HSIO_6            | X6              |
| 23  | PCIe x8 interface 7             | SW_HSIO_7            | X8              |
| 24  | Data communication interface    | LINK_SW              | X11             |
| 25  | PCIe x8 interface 8             | SW_HSIO_8            | X9              |
| 26  | PCIe x8 interface 9             | SW_HSIO_9            | X47             |
| 27  | PCIe x8 interface 10            | SW_HSIO_10           | X54             |
| 28  | PCIe x8 interface 11            | SW_HSIO_11           | X55             |
| 29  | Power interface 2               | P12V_SW2             | X13             |
| 30  | PCIe x8 interface 13            | SW_HSIO_13           | X48             |
| 31  | PCIe x8 interface 12            | SW_HSIO_12           | X10             |

### 9.3.3 SWP65N41A

Figure 9-5 shows the 21-slot PCIe 4.0 switch board SWP65N41A.

**Figure 9-5 SWP65N41A**



For a description of the interfaces on the 21-slot PCIe 4.0 switch board SWP65N41A, refer to [Table 9-5](#).

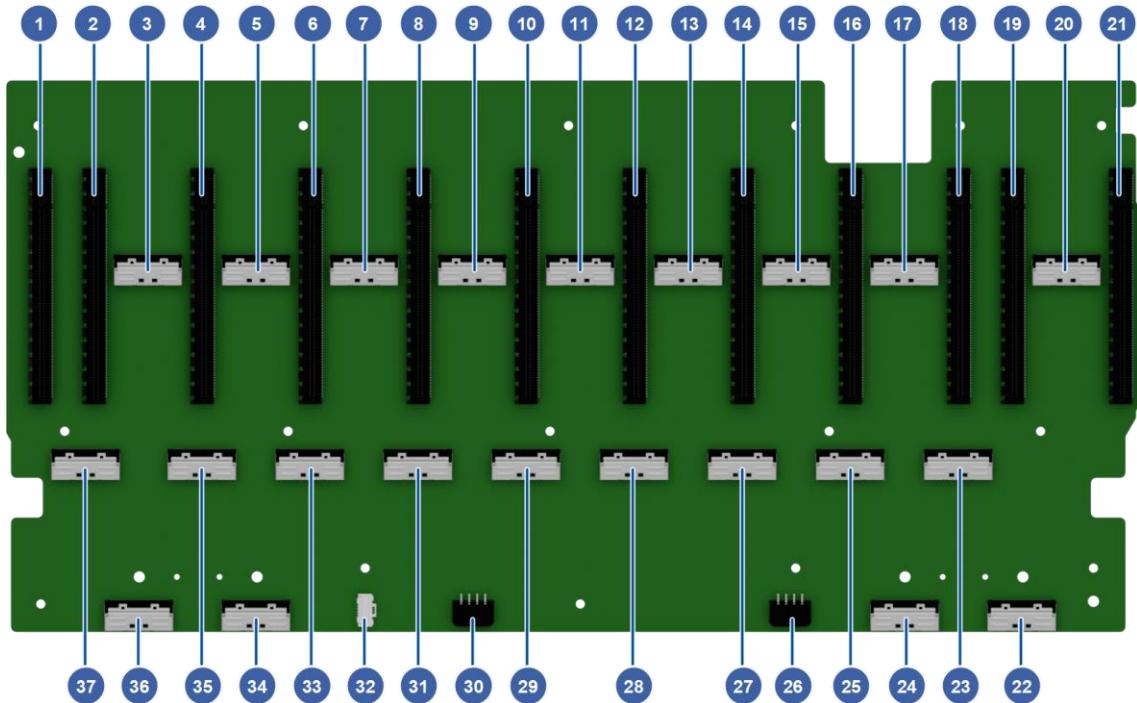
## Table 9-5 SWP65N41A Interface Descriptions

| No. | Interface Name    | Silk Screen | Position Number |
|-----|-------------------|-------------|-----------------|
| 1   | PCIe interface 21 | SLOT 21/X16 | X26             |
| 2   | PCIe interface 20 | SLOT 20/X16 | X25             |
| 3   | PCIe interface 19 | SLOT 19/X16 | X41             |
| 4   | PCIe interface 18 | SLOT 18/X16 | X40             |
| 5   | PCIe interface 17 | SLOT 17/X16 | X37             |
| 6   | PCIe interface 16 | SLOT 16/X16 | X36             |
| 7   | PCIe interface 15 | SLOT 15/X16 | X43             |
| 8   | PCIe interface 14 | SLOT 14/X16 | X42             |
| 9   | PCIe interface 13 | SLOT 13/X16 | X45             |
| 10  | PCIe interface 12 | SLOT 12/X16 | X44             |
| 11  | PCIe interface 11 | SLOT 11/X16 | X21             |

| No. | Interface Name                  | Silk Screen          | Position Number |
|-----|---------------------------------|----------------------|-----------------|
| 12  | PCIe interface 10               | SLOT 10/X16          | X20             |
| 13  | PCIe interface 9                | SLOT 9/X16           | C19             |
| 14  | PCIe interface 8                | SLOT 8/X16           | X18             |
| 15  | PCIe interface 7                | SLOT 7/X16           | X17             |
| 16  | PCIe interface 6                | SLOT 6/X16           | X16             |
| 17  | PCIe interface 5                | SLOT 5/X16           | X15             |
| 18  | PCIe interface 4                | SLOT 4/X16           | X14             |
| 19  | PCIe interface 3                | SLOT 3/X16           | X23             |
| 20  | PCIe interface 2                | SLOT 2/X16           | X22             |
| 21  | Smart NIC PCIe interface 1      | SLOT 1/PCIe GEN5/X16 | X24             |
| 22  | PCIe x8 interface 1             | SW_HSIO_1            | X7              |
| 23  | PCIe x8 interface 0             | SW_HSIO_0            | X73             |
| 24  | Power interface 1               | P12V_SW1             | X12             |
| 25  | Power interface 3               | P12V_GPU_SW3         | X70             |
| 26  | Smart NIC power cable interface | P12V_SMARTNIC        | X29             |
| 27  | PCIe x8 interface 2             | SW_HSIO_2            | X4              |
| 28  | PCIe x8 interface 3             | SW_HSIO_3            | X2              |
| 29  | PCIe x8 interface 4             | SW_HSIO_4            | X1              |
| 30  | PCIe x8 interface 5             | SW_HSIO_5            | X3              |
| 31  | Data communication interface    | LINK_SW              | X11             |
| 32  | PCIe x8 interface 6             | SW_HSIO_6            | X8              |
| 33  | PCIe x8 interface 7             | SW_HSIO_7            | X6              |
| 34  | PCIe x8 interface 8             | SW_HSIO_8            | X9              |
| 35  | PCIe x8 interface 9             | SW_HSIO_9            | X10             |
| 36  | Power interface 4               | P12V_GPU_SW4         | X71             |
| 37  | Power interface 2               | P12V_SW2             | X13             |

### 9.3.4 SW6505PT4A

Figure 9-6 shows the 12-slot PCIe 5.0 pass-through board SW6505PT4A.

**Figure 9-6 SW6505PT4A**

For a description of the interfaces on the 12-slot PCIe 5.0 pass-through board SW6505PT4A

**Table 9-6.****Table 9-6 SW6505PT4A Interface Descriptions**

| No. | Interface Name       | Silk Screen   | Position Number |
|-----|----------------------|---------------|-----------------|
| 1   | PCIe interface 13    | SLOT 13       | X38             |
| 2   | PCIe interface 12    | SLOT 12       | X37             |
| 3   | PCIe x8 interface 17 | CPU2_PE3_AB   | X21             |
| 4   | PCIe interface 11    | SLOT 11       | X36             |
| 5   | PCIe x8 interface 15 | CPU2_PE2_AB   | X20             |
| 6   | PCIe interface 10    | SLOT 10 PCIE5 | X35             |
| 7   | PCIe x8 interface 13 | CPU2_PE1_AB   | X16             |
| 8   | PCIe interface 9     | SLOT 9 PCIE5  | X34             |
| 9   | PCIe x8 interface 11 | CPU2_PE0_AB   | X17             |
| 10  | PCIe interface 8     | SLOT 8        | X33             |
| 11  | PCIe x8 interface 9  | CPU1_PE0_AB   | X13             |
| 12  | PCIe interface 7     | SLOT 7        | X32             |
| 13  | PCIe x8 interface 7  | CPU1_PE2_AB   | X14             |

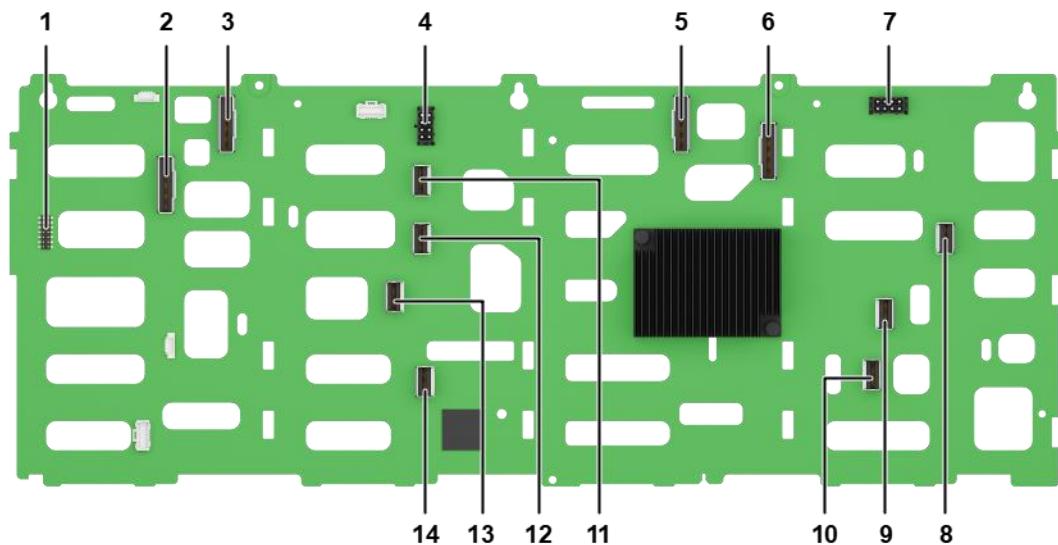
| No. | Interface Name               | Silk Screen  | Position Number |
|-----|------------------------------|--------------|-----------------|
| 14  | PCIe interface 6             | SLOT 6 PCIE5 | X31             |
| 15  | PCIe x8 interface 5          | CPU1_PE1_AB  | X9              |
| 16  | PCIe interface 5             | SLOT 5 PCIE5 | X30             |
| 17  | PCIe x8 interface 3          | CPU1_PE3_AB  | X8              |
| 18  | PCIe interface 4             | SLOT 4       | X29             |
| 19  | PCIe interface 3             | SLOT 3       | X28             |
| 20  | PCIe x8 interface 2          | CPU1_PE4_AB  | X6              |
| 21  | Smart NIC PCIe interface 1   | SLOT 1       | X27             |
| 22  | PCIe x8 interface 1          | CPU1_PE4_CD  | X5              |
| 23  | PCIe x8 interface 4          | CPU1_PE3_CD  | X10             |
| 24  | PCIe x8 interface 0          | CPU1_PE4_AB  | X7              |
| 25  | PCIe x8 interface 6          | CPU1_PE1_CD  | X11             |
| 26  | Power interface 1            | P12V_SW0     | X2              |
| 27  | PCIe x8 interface 8          | CPU1_PE2_CD  | X12             |
| 28  | PCIe x8 interface 10         | CPU1_PE0_CD  | X15             |
| 29  | PCIe x8 interface 12         | CPU2_PE0_CD  | X19             |
| 30  | Power interface 2            | P12V_SW1     | X3              |
| 31  | PCIe x8 interface 14         | CPU2_PE1_CD  | X18             |
| 32  | Data communication interface | LINK_SW      | X1              |
| 33  | PCIe x8 interface 16         | CPU2_PE2_CD  | X22             |
| 34  | PCIe x8 interface 21         | CPU2_PE4_CD  | X26             |
| 35  | PCIe x8 interface 18         | CPU2_PE3_CD  | X23             |
| 36  | PCIe x8 interface 20         | CPU2_PE4_AB  | X24             |
| 37  | PCIe x8 interface 19         | CPU2_PE4_AB  | X25             |

## 9.4 Disk Backplane

The NCS6742G N4 server supports the following types of disk backplanes:

- 24 x 3.5" disk backplane

[Figure 9-7](#) shows a 24 x 3.5" disk backplane.

**Figure 9-7 24 x 3.5" Disk Backplane**

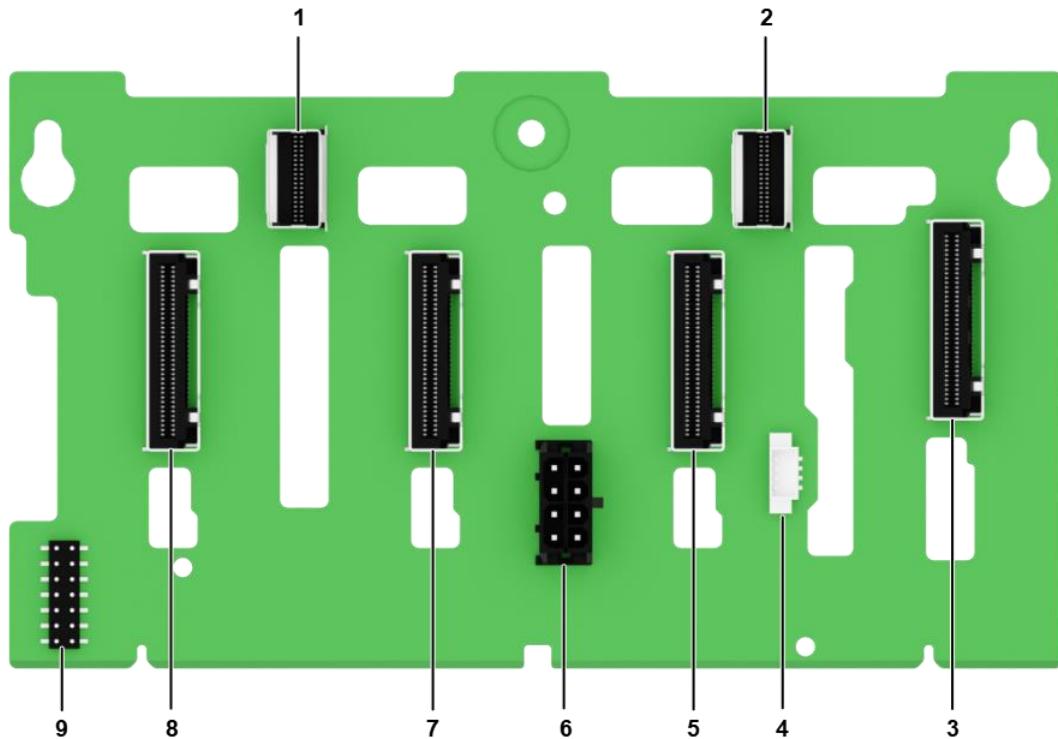
For a description of the interfaces on the 24 x 3.5" disk backplane, refer to [Table 9-7](#).

**Table 9-7 Interfaces on the 24 x 3.5" Disk Backplane**

| No. | Interface Name                              | Silk Screen           | Position Number |
|-----|---|-----------------------|-----------------|
| 1   | JTAG programming interface of the EPLD chip | EPLD_JTAG             | X45             |
| 2   | PCIe x8 interface 4                         | NVMe SLIMLINE4        | X5              |
| 3   | PCIe x8 interface 3                         | NVMe SLIMLINE3        | X3              |
| 4   | Power cable interface 2                     | PWR2                  | X2              |
| 5   | PCIe x8 interface 2                         | NVMe SLIMLINE2        | X31             |
| 6   | PCIe x8 interface 1                         | NVMe SLIMLINE1        | X30             |
| 7   | Power cable interface 1                     | PWR1                  | X1              |
| 8   | Downlink PCIe x4 interface 4                | RISER HDD BP/SLIMSAS4 | X40             |
| 9   | Downlink PCIe x4 interface 5                | HDD BP/SLIMSAS5       | X36             |
| 10  | Downlink PCIe x4 interface 6                | HDD BP/SLIMSAS6       | X37             |
| 11  | Uplink PCIe x4 interface 1                  | SLIMSAS1              | X34             |
| 12  | Uplink PCIe x4 interface 2                  | SLIMSAS2              | X35             |
| 13  | Downlink PCIe x4 interface 3                | RISER HDD BP/SLIMSAS3 | X39             |
| 14  | Downlink PCIe x4 interface 7                | HDD BP/SLIMSAS7       | X38             |

- 8 x 2.5" disk backplane

[Figure 9-8](#) shows an 8 x 2.5" disk backplane.

**Figure 9-8 8 x 2.5" Disk Backplane**

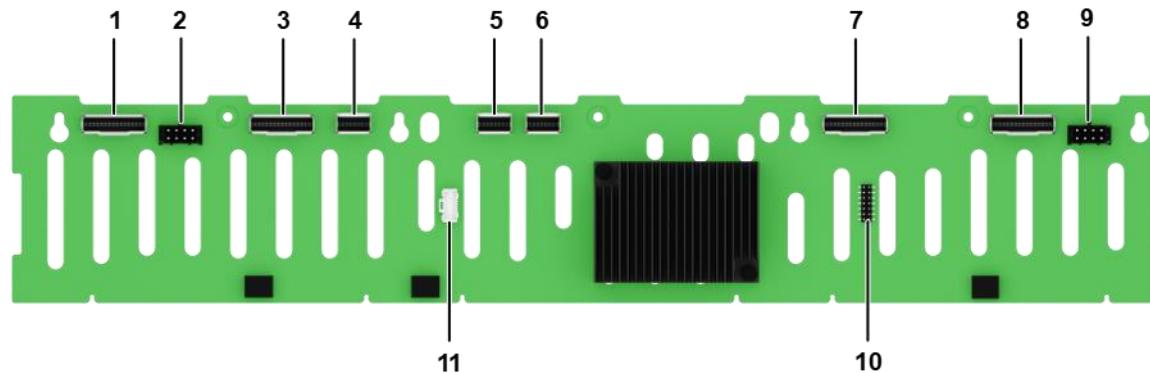
For a description of the interfaces on the 8 x 2.5" disk backplane, refer to [Table 9-8](#).

**Table 9-8 Interfaces on the 8 x 2.5" Disk Backplane**

| No. | Interface Name                              | Silk Screen | Position Number |
|-----|---|-------------|-----------------|
| 1   | PCIe x4 interface                           | SAS_2       | X15             |
| 2   | PCIe x4 interface                           | SAS_1       | X14             |
| 3   | PCIe x8 interface                           | HSIO_1      | X10             |
| 4   | Out-of-band communication interface         | I2C 1       | X17             |
| 5   | PCIe x8 interface                           | HSIO_2      | X11             |
| 6   | Power cable interface                       | PWR 1       | X16             |
| 7   | PCIe x8 interface                           | HSIO_3      | X12             |
| 8   | PCIe x8 interface                           | HSIO_4      | X13             |
| 9   | JTAG programming interface of the EPLD chip | CPLD_JTAG   | X305            |

- 25 x 2.5" disk backplane

[Figure 9-9](#) shows a 25 x 2.5" disk backplane.

**Figure 9-9 25 x 2.5" Disk Backplane**

For a description of the interfaces on the 25 x 2.5" disk backplane, refer to [Table 9-9](#).

**Table 9-9 Interfaces on the 25 x 2.5" Disk Backplane**

| No. | Interface Name                              | Silk Screen  | Position Number |
|-----|---|--------------|-----------------|
| 1   | PCIe x8 interface                           | SLIMLINE_4   | X34             |
| 2   | Power cable interface                       | PWR_2        | X5              |
| 3   | PCIe x8 interface                           | SLIMLINE_3   | X33             |
| 4   | PCIe x4 interface                           | SLIMSAS_3    | X37             |
| 5   | PCIe x4 interface                           | SLIMSAS_2    | X35             |
| 6   | PCIe x4 interface                           | SLIMSAS_1    | X36             |
| 7   | PCIe x8 interface                           | SLIMLINE_2   | X32             |
| 8   | PCIe x8 interface                           | SLIMLINE_1   | X31             |
| 9   | Power cable interface                       | PWR_1        | X4              |
| 10  | JTAG programming interface of the EPLD chip | CPLD_JTAG    | X30a11          |
| 11  | Out-of-band communication interface         | I2C/SPI/UART | X38             |

# Chapter 10

# Cables

## Table of Contents

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## 10.1 Power Cables

The NCS6742G N4 is configured with different power supply modules to provide [AC](#) or [DC](#) power supply. In accordance with the power distribution condition, an AC power supply module can use an AC power cable with a three-flat-pin male plug or with pre-insulated tubular terminals, and a DC power supply module can use a high-voltage DC power cable or -48 V DC power cable.

### 10.1.1 AC Power Cable with a Three-Flat-Pin Male Plug

#### Function

An AC power cable with a three-flat-pin male plug is connected to a power strip in the cabinet to supply power for the NCS6742G N4 server chassis.

#### External View

[Figure 10-1](#) shows an external view of an AC power cable with a three-flat-pin male plug.

[Figure 10-1 AC Power Cable with a Three-Flat-Pin Male Plug](#)



End A of the power cable is a C13 female connector, and end B is a 10 A three-flat-pin male plug. The power cable is a black AC power cable.

## Connections

For the connections of an AC power cable with a three-flat-pin male plug, refer to [Table 10-1](#).

**Table 10-1 Connections of an AC Power Cable with a Three-Flat-Pin Male Plug**

| End A  | End B                                      |
|--|--|
| Connected to the power input port of an AC PSU on the chassis. | Connected to a power strip in the cabinet. |

## Technical Specifications

- Rated current: 10 A.
- Internal wires: three wires, each with a cross-sectional area of 1 mm<sup>2</sup>.

### 10.1.2 AC Power Cable with Pre-Insulated Tubular Terminals

#### Function

An AC power cable with pre-insulated tubular terminals is connected to the AC PDU in the equipment room to supply power for the NCS6742G N4 server chassis.

#### External View

[Figure 10-2](#) shows an external view of an AC power cable with pre-insulated tubular terminals.

**Figure 10-2 AC Power Cable with Pre-Insulated Tubular Terminals**



End A of the power cable is a C13 female connector, and end B consists of pre-insulated tubular terminals. The power cable is a black AC power cable.

For the correspondence between the wires and pins of an AC power cable with pre-insulated tubular terminals, refer to [Table 10-2](#).

**Table 10-2 Correspondence Between Wires and Pins of an AC Power Cable with Pre-Insulated Tubular Terminals**

| Pin of End A | Wire Color   | Pin of End B |
|--------------|--------------|--------------|
| L            | Brown        | B1           |
| N            | Blue         | B2           |
| E            | Yellow-green | B3           |

## Connections

For the connections of an AC power cable with pre-insulated tubular terminals, refer to [Table 10-3](#).

**Table 10-3 Connections of an AC Power Cable with Pre-Insulated Tubular Terminals**

| End A  | End B                                     |
|--|---|
| Connected to the power input port of an AC PSU on the chassis. | Connected to the AC <a href="#">PDU</a> . |

## Technical Specifications

- Rated current: 10 A.
- Internal wires: three wires, each with a cross-sectional area of 1 mm<sup>2</sup>.

### 10.1.3 HVDC Power Cable

#### Function

An [HVDC](#) power cable is connected to the [DC PDU](#) in the equipment room to supply power for the NCS6742G N4 server chassis.

#### External View

[Figure 10-3](#) shows an external view of an HVDC power cable.

**Figure 10-3 HVDC Power Cable**



End A of the power cable is an HVDC female connector, and end B consists of pre-insulated tubular terminals. The power cable is a black DC power cable.

For the correspondence between the wires and the pins of the HVDC power cable, refer to [Table 10-4](#).

**Table 10-4 Correspondence Between the Wires and Pins of an HVDC Power Cable**

| Pin of End A | Wire Color   | Pin of End B |
|--------------|--------------|--------------|
| L (+)        | Brown        | B1           |
| N (-)        | Blue         | B2           |
| FG           | Yellow-green | B3           |

## Connections

For the connections of an HVDC power cable, refer to [Table 10-5](#).

**Table 10-5 Connections of an HVDC Power Cable**

| End A   | End B  |
|---|--|
| Connected to the power input port of a DC PSU of the chassis. | Connected to the DC PDU in the equipment room. |

## Technical Specifications

- Rated current: 10 A.
- Internal wires: three wires, each with a cross-sectional area of 1 mm<sup>2</sup>.

### 10.1.4 -48 V DC Power Cable

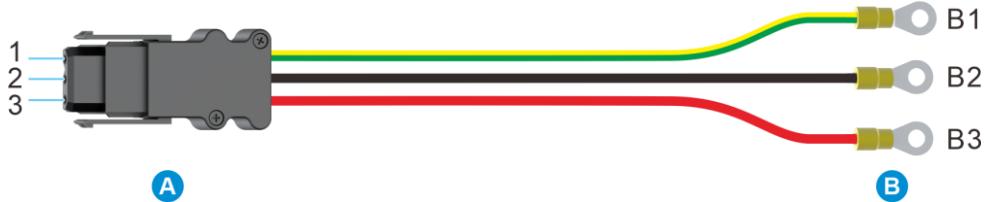
#### Function

A -48 V DC power cable is connected to the DC PDU in the equipment room to supply power for the NCS6742G N4 server chassis.

#### External View

[Figure 10-4](#) shows an external view of a -48V DC power cable.

**Figure 10-4 -48V DC Power Cable**



End A of the power cable is a dedicated -48 V DC power plug, and end B consists of pre-insulated terminals with copper lugs. The power cable has three wires: one red wire, one black wire, and one yellow-green wire.

For the correspondence between the wires and pins of the -48 V DC power cable, refer to [Table 10-6](#).

**Table 10-6 Correspondence Between the Wires and Pins of a -48V DC Power Cable**

| Pin of End A | Wire Color   | Pin of End B         |
|--------------|--------------|----------------------|
| 1            | Yellow-green | B1 (label: PE)       |
| 2            | Black        | B2 (label: -48 V)    |
| 3            | Red          | B3 (label: -48 VRTN) |

## Connections

For the connections of a –48 V DC power cable, refer to [Table 10-7](#).

**Table 10-7 –48 V DC Power Cable Connections**

| End A   | End B  |
|---|--|
| Connected to the power input port of a DC PSU of the chassis. | Connected to the DC PDU in the equipment room. |

## Technical Specifications

Rated current: 26 A.

## 10.2 Straight-Through Cable

### Function

A straight-through cable is used to connect two devices or terminals for data transmission.

### External View

[Figure 10-5](#) shows an external view of a straight-through cable.

**Figure 10-5 Straight-Through Cable**



End A and end B of a shielded straight-through cable are shielded 8P8C crimped plugs. End A and end B of a non-shielded straight-through cable are non-shielded 8P8C crimped plugs.

The main differences between shielded and unshielded straight-through cables lie in the structures, resistance to interference, and application scenarios.

- **Shielded straight-through cable:** This type of cable contains a metal shielding layer to reduce electromagnetic interference and RF interference, thus increasing signal quality and transmission distance. Shielded straight-through cables are typically used in environments with high data transmission requirements, such as data centers or industrial automation settings.
- **Unshielded straight-through cable:** This type of cable lacks an additional metal shielding layer, resulting in lower resistance to interference. Due to its lower cost and ease of installation, unshielded straight-through cables are widely used in home and office environments.

## Connections

The two ends of a straight-through cable are connected to the network interfaces (RJ45 interfaces) of the devices or terminals that require data transmission.

## Technical Specifications

A shielded straight-through cable is an eight-core 100-ohm Cat5e shielded cable. An unshielded straight-through cable is an eight-core 100-ohm Cat5e unshielded cable. [Table 10-8](#) describes the correspondence between cores.

**Table 10-8 Correspondence Between Wires and Pins of a Straight-Through Cable**

| End A | Color        | End B |
|-------|--------------|-------|
| 1     | White-orange | 1     |
| 2     | Orange       | 2     |
| 3     | White-green  | 3     |
| 4     | Blue         | 4     |
| 5     | White-blue   | 5     |
| 6     | Green        | 6     |
| 7     | White-brown  | 7     |
| 8     | Brown        | 8     |



### Note

The metal shielding layer of a shielded cable must be securely connected to the metal shielding enclosures of connectors at both ends.

## 10.3 Serial Cable

### Function

A serial cable connects the serial port on the NCS6742G N4 chassis to the serial port of a debugging [PC](#).

### External Overview

[Figure 10-6](#) shows an external view of a serial cable.

**Figure 10-6 Serial Cable**

End A of a serial cable is a 3.5 mm audio plug, and end B is a 9-pin D-shape molded plug. Both end A and end B are numbered as pin numbers.

### Connections

For a description of the connections of a serial cable, refer to [Table 10-9](#).

**Table 10-9 Serial Cable Connections**

| End A   | End B  |
|---|--|
| Connected to the 3.5 mm audio port of the server. | Connected to the <a href="#">RS-232</a> debugging serial port (DB9) of a debugging PC. |

### Technical Specifications

For the correspondence between the pins of the connectors at both ends of the serial cable, refer to [Table 10-10](#).

**Table 10-10 Correspondence Between Pins on Both Ends of the Serial Cable**

| Pin at End A | Pin at End B |
|--------------|--------------|
| 1            | 2            |
| 2            | 3            |
| 3            | 5            |
| 4            |              |

## 10.4 VGA Cable

### Function

A [VGA](#) cable is used to connect the NCS6742G N4 and a media display.

### External Overview

[Figure 10-7](#) shows the external overview of a VGA cable.

**Figure 10-7 VGA Cable**

A VGA cable is a beige UL2919 cable with magnetic rings, and uses HD-SUB plugs at both ends.

### Connections

For the connections of a VGA cable, refer to [Table 10-11](#).

**Table 10-11 VGA Cable Connections**

| End A  | End B  |
|--|--|
| Connected to the VGA interface on the chassis. | Connected to the VGA interface of a media display. |

### Technical Specifications

A VGA cable is a horizontal pair-twisted cable. For the correspondence between the wires and pins of a VGA cable, refer to [Table 10-12](#).

**Table 10-12 Correspondence Between the Wires and Cores of a VGA Cable**

| End A | Color                            | End B |
|-------|----------------------------------|-------|
| 1     | Core of the red cord             | 1     |
| 2     | Core of the gray cord            | 2     |
| 3     | Core of the blue cord            | 3     |
| 4     | (Blank)                          | 4     |
| 5     | External shielded wire           | 5     |
| 6     | Core of the red cord             | 6     |
| 7     | Core of the gray cord            | 7     |
| 8     | Core of the blue cord            | 8     |
| 9     | (Blank)                          | 9     |
| 10    | Shielded wire for the white cord | 10    |
| 11    | Shielded wire for the black cord | 11    |
| 12    | Black wire                       | 12    |
| 13    | Shielded wire for the white cord | 13    |
| 14    | Shielded wire for the black cord | 14    |

---

| End A | Color      | End B |
|-------|------------|-------|
| 15    | Brown wire | 15    |

---



The external shielded wire for the entire VGA cable, shielded wire for the white cord, and shielded wire for the black cord are connected and grounded together through the VGA plug shell.

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# Chapter 11

## Anti-Intrusion Sensor

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The functions of the anti-intrusion sensor are as follows:

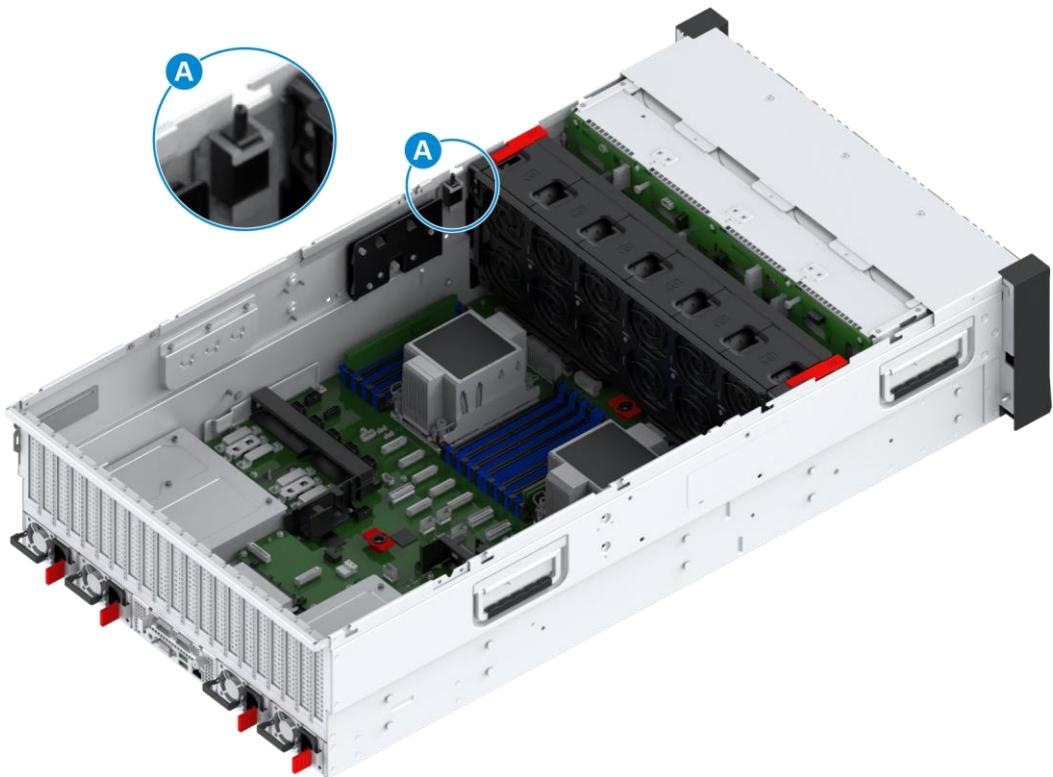
- Triggers an alarm to indicate that the cover of the server is not installed or is not installed properly.
- Ensures good heat dissipation of related components and proper operation of the server if the cover of the server is not installed or is not installed properly.

When the server is in power-on status, once the anti-intrusion sensor detects that the cover is open, it triggers the following actions:

- The [BMC](#) reports a system intrusion alarm, indicating that the cover of the server is not installed or is not installed properly.
- The fans of the server operate at the maximum speed to ensure good heat dissipation.

[Figure 11-1](#) shows the position of the anti-intrusion sensor in the NCS6742G N4 server.

[Figure 11-1 Position of the Anti-Intrusion Sensor](#)



# Glossary

---

## **AC**

- Alternating Current

## **ADDDC**

- Adaptive Double Device Data Correction

## **BIOS**

- Basic Input/Output System

## **BMC**

- Baseboard Management Controller

## **CAS**

- Column Address Strobe

## **CPU**

- Central Processing Unit

## **CRC**

- Cyclic Redundancy Check

## **DC**

- Direct Current

## **DDR**

- Double Data Rate

## **DIMM**

- Dual Inline Memory Module

## **DRAM**

- Dynamic Random Access Memory

## **ECC**

- Error Check and Correction

**ECS**

- Error Check and Scrub

**EPLD**

- Erasable Programmable Logic Device

**GPU**

- Graphics Processing Unit

**HBM**

- High Bandwidth Memory

**HVDC**

- High-Voltage Direct Current

**I/O**

- Input/Output

**JTAG**

- Joint Test Action Group

**NIC**

- Network Interface Card

**NVMe**

- Non-Volatile Memory Express

**OCP**

- Open Computer Project

**OS**

- Operating System

**PC**

- Personal Computer

**PCH**

- Platform Controller Hub

**PCIe**

- Peripheral Component Interconnect Express

**PCLS**

- Partial Cache Line Sparing

**PDU**

- Power Distribution Unit

**PPR**

- Post-Package Repair

**RAID**

- Redundant Array of Independent Disks

**RDIMM**

- Registered Dual Inline Memory Module

**RS-232**

- Recommended Standard 232

**SAS**

- Serial Attached SCSI

**SATA**

- Serial ATA

**SDDC**

- Single Device Data Correction

**SPD**

- Serial Presence Detect

**TPM**

- Trusted Platform Module

**UID**

- Unit Identification Light

**UPI**

- Ultra Path Interconnect

**USB**

- Universal Serial Bus

**VGA**

- Video Graphic Adapter